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OPERATIONAL SIMULATION OF AN X-RAY LITHOGRAPHY CELL: COMPARISON OF 200MM AND 300MM WAFERS

K. Preston White, Jr.

Department of Systems Engineering
University of Virginia Institute for Microelectronics
University of Virginia
Charlottesville, VA 22903-2442

Walter J. Trybula

International SEMATECH, Inc.
2706 Montopolis Drive
Austin, TX 78741-6499

ABSTRACT

We review progress on a project to evaluate prospective operations in a semiconductor wafer fab that employs next-generation, proximity X-ray lithography to pattern the critical dimensions of computer chips. A simulation model is developed that captures the processing of wafers through an X-ray lithography cell using a synchrotron as the source of exposure radiation. The model incorporates the best current information on unit-cell design and processing times and implements a range of events that interrupt the flow of wafers processing on the cell. Performance measures estimated from the simulation include the weekly throughput for the cell and the frequency of SEMI E-10 equipment states for the corresponding exposure tool. Simulation experiments are conducted to compare the performance of a cell fabricating 200mm wafers with that of a cell fabricating 300mm wafers, for each of three different chip sizes. Results illustrate the anticipated dependence of average wafer throughput on wafer size and assumptions regarding the number of chips per wafer, with a maximum of approximately 3400 wafers/week for 200mm wafers with 25x25mm field size. Ignoring wafer-sort losses, however, a maximum throughput of approximately 410,000 chips/week is realized for 300mm wafers with 11x22mm fields. Remarkably, the distribution of equipment states remains relatively unchanged across simulation experiments.

1 INTRODUCTION

Projected to reach commercial production in memory chips around the year 2001, next-generation semiconductor devices will realize integrated circuits with critical dimensions at 130nm and below (SIA 1999). These small geometries are approaching the practical limits of resolution using industry-standard optical lithography (El-Kareh 1995; Van Zant 1997). While optical lithography certainly will continue as the mainstay for non-critical mask levels, imaging the minimum feature sizes of future next-generation devices ultimately will require an advanced lithography technology employing an exposure beam with wavelength shorter than 193nm ArF deep ultraviolet light (DUV).

Alternatives under development for post-optical lithography include proximity X-ray, E-beam projection, E-beam direct write, extreme ultraviolet (EUV), and ion projection technologies. Among these, X-ray proximity lithography has had the most resources applied to its development, both in the United States and Japan (SIA 1997). Significant scientific and technological advances have been demonstrated for X-ray lithography over the past two decades (Mizusawa *et al.* 1997). In particular, researchers at the IBM Advanced Lithography Facility (ALF) have reported encouraging results in tests of the reliability of synchrotron storage rings and associated subsystems as a source of X-rays for semiconductor lithography (Andrews *et al.* 1990; Lesoine *et al.* 1990; Lesoine and Kukkonen 1992; Andrews and Archie 1993; Archie 1993; Silverman *et al.* 1993). While the ability to manufacture large-area, defect-free, 1x masks looms as a potential "show-stopper" for volume production, X-ray nevertheless remains a serious candidate for next-generation lithography (Mizusawa *et al*. 1997).

For several years we have been investigating the impact on the factory floor of using a synchrotron as the key element in lithography systems for patterning critical levels in commercial semiconductor fabs (White and Trybula 1997, 1999). The size, cost, and unique operating characteristics of synchrotron technology, together with the configuration of lithography areas in which a single ring is the source of multiple-beams for perhaps as many as 25 critical-level steppers, give rise to a range of tool availability and utilization issues. These issues are considerably more complex than those encountered in production using conventional optical lithography. If

fundamental technological challenges to proximity X-ray are overcome, the resolution of these operational issues is essential for the efficient and effective design, layout, start-up, and management of the next generation of semiconductor fabs.

Aspects of the cost of ownership for X-ray proximity have been addressed admirably by Wilson (1986), Hill (1989), Kovacs *et al.* (1990), and Early and Arnold (1994). These cost analyses are static, however, and do not incorporate the dynamics of planning, scheduling, and operating X-ray lithography cells to produce chips with geometries at or below 130nm. Actual cycle times are likely to be greater, and throughput and production efficiencies smaller, when dynamic issues are taken into account.

As an illustration, consider a new fab designed for 5000 200-mm wafer starts per week, running both high- and low-volume products, using the 0.18μm-copper-interconnect process described by Catalano, *et al.* (1997). This process incorporates over 454 individual steps, requiring 21 lithography levels, of which 5 levels have critical dimensions of 180-220nm. The complex, multiple-reentrant flow of different wafer types through alternate lithography areas already constitutes a challenging queuing, scheduling, and tracking problem for wafers in production. Scheduling is made more complicated by the need to inspect and accept, reject, repair, or reprocess wafers after key processing steps; by overlay problems associated with decisions to mix and match different lithography tools; and by the desire to maintain maximum utilization of the most expensive lithography tools.

With critical levels employing synchrotron-based X-ray lithography at 130nm and below, the picture is further confounded. Beam availability to *all* critical tools connected to a common synchrotron ring depends on resist and process latitudes and on time-varying beam intensity. Beam lifetime and recharge duration in turn depend on available injection energy to the ring. Scheduled and unscheduled maintenance is required for sensitive equipment, some of which is common to all tools and some of which is tool specific. Finally, the cost and service life of critical masks remain key, unresolved issues.

In this paper we review progress on a project to evaluate the future implementation of X-ray lithography. The purpose of this project is to develop the operational modeling and analysis tools required to evaluate, schedule, and optimize the performance of X-ray lithography cells based on quantitative measures of manufacturing productivity. To this end, we have developed and applied a simulation model that represents the processing of wafers through an advanced X-ray lithography cell employing a single synchrotron ring as the source of exposure radiation.

Section 2 describes the cell model and wafer processing assumptions. Subsequent sections define the arrival logic and queuing discipline for cassettes and cassette trains; the logic for the inspection and rework process; the logic for processing test wafers; and the logic for downtime and engineering equipment states. The experiment design is presented in Section 8 and Section 9 reports and analyzes the results of these experiments. Conclusions are offered in the final section.

2 SIMULATION MODEL

The process flow model for the X-ray lithography unit cell is shown in Figure 1. The cell comprises 15 modules. Wafers are primed and coated with a single layer of resist on the pre-exposure track, open to the atmosphere. Pre-alignment and exposure operations are contained within a reduced atmosphere of helium, accessed through a single loadlock. Wafers are developed and etched on the post-exposure track, also open to the atmosphere. Estimates for processing and transfers times for each of the component modules appear on the figure. Note that the layout of the X-ray lithography area depicted in Figure 1 is strictly hypothetical, intended only to suggest the principle modules their general interrelationships.

The unit cell is an example of a queuing system called a *transfer line*. Modules on the cell have unit capacity and each module can process only one wafer at a time. Without buffers between the modules, wafers that complete processing at one module are blocked from entering the next downstream module until the downstream module is free. By design, the exposure tool gates or paces the cell during normal production with a minimum processing time of 101 sec/wafer. Reentrance at loadlock, which must be accessed both before and after exposure, complicates the otherwise linear process flow.

A synchrotron ring provides exposure radiation to the cell through a beam tube connecting at the exposure tool. Dedicated rework and inspection stations support the cell. The cell also includes dedicated WIP storage for arriving and departing cassette trains.

3 ARRIVAL PROCESS/CASSETTE QUEUEING

It is assumed that wafers arrive at the X-ray lithography area in lots (called *trains*) comprising multiple cassettes. All of the wafers in a train, regardless of cassette, are of the same product type at the same process level. The deployment of cassette trains is motivated by the need to reduce the number of setups on the cell and the attending adverse impact of setups on wafer throughput and equipment utilization. In the baseline model, there are twenty-five 200mm-wafers per cassette. Because of the greater weight of the larger wafers, in the alternate model there are only twelve 300-mm wafers per cassette. In both cases, the train length is randomly distributed according to a discrete uniform distribution with a minimum of five and

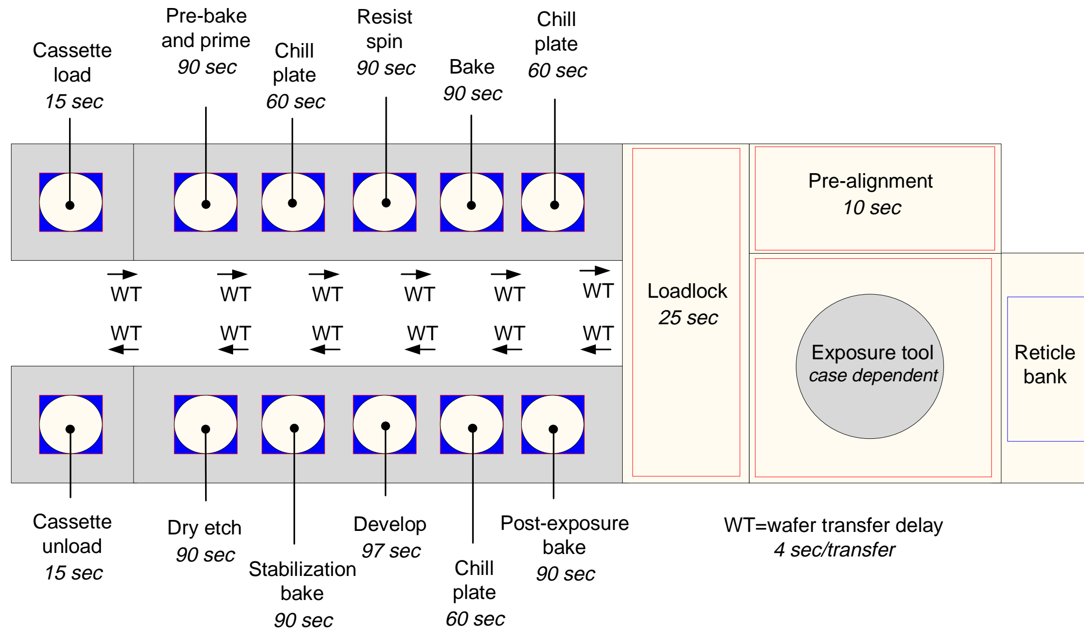

Figure 1: Schematic of Process Flow on an X-Ray Lithography Unit-Cell with Processing Parameters

a maximum of nine cassettes, for an average of seven cassettes per train.

For this work, it is assumed that there is only one product type actively in production. This product has five different mask levels at the critical dimension (active area, gate, contact, metal 1, and via 1). It is assumed that wafers at each critical level arrive at the X-ray cell in equal proportions over the long term, with no significant fallout between levels. The order in which cassette trains arrive at the X-ray area is randomly distributed with respect to process level, according to a discrete uniform distribution. (Future work will look at more exact process flows as these become available.)

Cassette trains wait in a common queue at the X-ray lithography input WIP area for processing on the next free cell. Train queuing is first-in-first-out (FIFO), without regard to matching process level between successive trains processed on the same cell. The process level for the wafers in each train is randomly reassigned at the beginning of each train cycle.

Each train completes processing entirely on the cell before the cell is free to process next train. For this reason, there is always standby/idle time on the exposure tool between successive trains, incurred while the post-exposure track and inspection module clear the final wafers in the final cassette within each train. An additional delay can occur if any rework is incomplete on wafers in the departing train.

Within trains, cassettes wait in a common queue for processing on the cell. Each cassette begins processing on the cell immediately after the last wafer in the preceding cassette within the same train frees the cassette-unload module. The launching of wafers between cassettes within the same train is not delayed by rework. Cassette queuing is FIFO within train.

A fundamental assumption is that an advanced wafer fab is operated such that there is always WIP waiting to be processed at the critical lithography tools. Under this assumption, the X-ray cell is never starved during normal operation. Although impossible achieve absolutely, this objective is consistent with the economic operation of an advanced wafer fab and is assumed to be achieved approximately.

This fundamental assumption is implemented in the simulation by recycling a finite number of cassette trains (in excess of the total capacity of the cell) through the X-ray lithography area. From a modeling perspective, this has the advantage of obviating the need to balance area interarrival times and cycle times *a priori*. The number of wafer starts is determined implicitly within the model, based on the dynamic capacity of the entire lithography area. Within the simulation model, this artifice also guarantees that queues are stable and cells are never starved.

This fundamental assumption implies that the simulation results for the X-ray cell are essentially independent of operations external to the cell and that results are scaleable to any number of cells operating on any number of rings within the critical lithography area. A potential exception to the scalability assumption occurs during the clearing of the cell prior to beam charge and ring preventive maintenance (PM). It is assumed that scheduled

maintenance does not begin until all of the cells are cleared through the exposure tool. Thus, with larger the numbers of cells attached to the same ring, it is more likely that some of the cells are fully loaded on the pre-exposure track, while others are partially loaded or empty. This will tend to increase the average standby/idle time for cell clearing experienced by all cells attached to a common ring. The extent of this additional standby/idle time during clearing should be very small, given the relative infrequency of beam charges, and should approach the maximum processing time on the pre-exposure track in the limit as a function of increasing the population of cells on a ring.

4 INSPECTION AND REWORK PROCESSES

It is assumed there is one inspection station for each lithography cell and that wafers undergo 100% inspection. Inspection times are randomly distributed according to a continuous normal distribution with a mean of 2 minutes and a standard deviation of 0.25 minutes. The inspection station has the capacity to process at most two wafers simultaneously. A wafer passes inspection with probability 0.99, independently of process level.

If a wafer fails inspection, it is reworked and returned as the last wafer in the current input cassette for its assigned cell. It is assumed that there is one rework station for each lithography cell. Rework time is 5 minutes per wafer. The inspection and reworking of a wafer or wafers from one cassette does not preclude the launch of wafers from a successor cassette, if the successor cassette is a member of the same train. On the other hand, if the next wafer belongs to a cassette within a new train, the inspection and reworking of a wafer or wafers from one cassette blocks the launch of all wafers from a successor until the rework is complete and passes inspection.

5 SEND-AHEAD WAFER

A *test* or *send-ahead wafer* (SAW) is launched when the product-type and/or process level of wafers in next cassette differs from that of wafers in the preceding cassette. Under the assumption of a single product type, therefore, a SAW must be launched and pass inspection for each cassette train, if and only if successor trains differ in process level. A SAW is not required for a partial cassette that continues processing after downtime or engineering.

The initial SAW in a cassette train waits for reticle changeover before it is launched. The reticle changeover time is uniformly continuously distributed with a minimum of 20 and a maximum of 30 sec. A SAW completes processing on the entire cell and is inspected before the next wafer is launched. If a SAW fails inspection, the next wafer in the current cassette is launched as a new SAW after a delay for reticle adjustment. The reticle adjustment times are the same as reticle changeover times. If a SAW fails inspection, it is reworked and returned as the last wafer in the current input cassette.

6 EQUIPMENT STATES

The SEMI E-10 guidelines (Konopka, J. 1993; Trybula and Pratt 1994) provide an accepted standard for the description and classification of equipment states. These guidelines were established by the semiconductor industry in order to collect, analyze, and apply information from equipment regarding its operating condition. As shown Figure 2, the SEMI E-10 guidelines define six equipment states at the most basic descriptive level.

Nonscheduled time occurs when a piece of equipment is not scheduled for any type of normal or maintenance operations. Equipment downtime includes both unscheduled and scheduled downtime. *Unscheduled downtime* is any time when equipment is not capable of performing its function, because of an undesired condition, such as a failure, or because required consumables are unavailable. *Scheduled downtime* occurs during any planned outage, including PM and scheduled changing of consumables.

Equipment is in one of the uptime states if it is available for use in production or production-related activities. *Engineering* occurs during time scheduled for process or engineering work. *Standby/idle* is a catchall category that includes time spent awaiting parts, awaiting test results, or even awaiting an operator to start the tool. *Productive* time is the actual time the equipment is running production material for planned requirements.

In the simulation model, equipment states are recorded and reported for each exposure tool, as a surrogate for the corresponding lithography cell. The six basic SEMI E-10 equipment states are mapped onto the expanded set of simulated equipment states for the exposure tools as shown in Figure 2 and defined inTable 1. The expanded set of simulated equipment states provides greater detail on the sources of exposure-tool idleness.

7 DOWNTIMES

7.1 Scheduled Downtimes

Scheduled downtimes include downtime for beam recharge, cell PM, and ring PM. Scheduled downtime sequences begin by clearing wafers in process on the track and the exposure tool. Anticipating the downtime in this way avoids rework of partially processed wafers and adverts the likely consequence of reduced yields resulting from such rework. Wafers that have not begun processing at the start of a scheduled downtime sequence are held in the input cassette. Wafers that have completed processing prior to the scheduled downtime sequence, or that are cleared during the beginning of the current the sequence, are held in the output cassette.

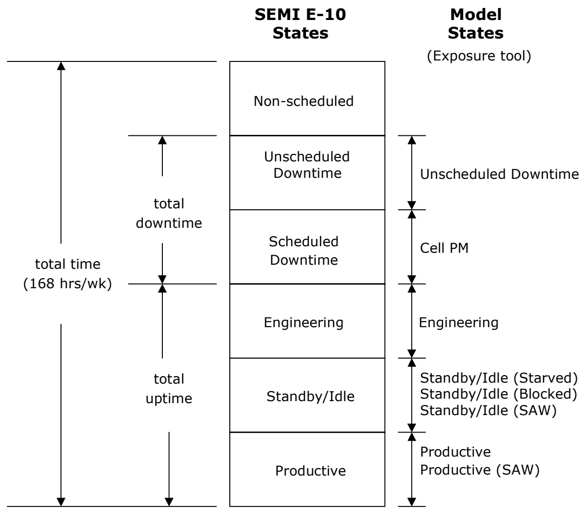

Figure 2: SEMI E-10 Guidelines Applied To The X-Ray Lithography Model Equipment States

For cell PM, wafers are cleared completely through the cell prior to shutdown of the entire cell. For beam charge and ring PM, wafers are cleared through the pre-exposure track and the exposure tool prior to shutdown of the exposure tool. Wafers initiated prior to beam charge and ring PM, therefore, complete processing on post-exposure track and inspection station while the exposure tool is shut down or is awaiting shutdown.

If the exposure tool and all eight of the track modules upstream of the stepper are busy processing wafers when we begin to prepare for shutdown, it takes a maximum of 12.2 min (at the maximum exposure time) for the cell to clear as described. This is approximately 2.5% of the average 480-min delay between recharges for a 500ma charge, which does not appear to cause a significant variation from the downtime schedule.

At 500 ma, initiation of the beam recharge sequence is normally distributed with a mean of 480 min (8 hrs) and a standard deviation of 30 min during normal operation. Beam recharge requires 15 min. Beam recharge can occur simultaneously while a cell is undergoing PM, in which case the state of the system is accounted as cell PM. Beam recharge is assumed to be the last step in ring PM and the ring comes up charged after PM sequence.

The cell PM sequence is initiated once every 1440 min (24 hrs) and requires 45 min. The ring PM sequence is initiated once every 10080 min (1 wk) and requires 480 min (8 hrs). Cell PM can occur simultaneously with ring PM and the cell comes up freshly maintained after ring PM. Unscheduled downtime does not delay initiation of cell or ring PM. A cell can undergo simultaneous unscheduled downtime scheduled downtime for ring PM, if the unscheduled downtime is initiated prior to scheduled downtime. The state of a cell undergoing simultaneous unscheduled and scheduled downtime for ring PM is accounted as unscheduled downtime for the duration of the failure.

Table 1: Relationship Between SEMI E-10 States and Simulation Output States

SEMI E-10 state	**Simulation state**	**Note**
Nonscheduled		Not modeled
Unscheduled downtime	Unsched Downtime	Cell failure at exposure tool or on track, recorded as exposure-tool downtime from initiation of incident
Scheduled downtime	SD_CellPM	Cell PM, recorded as exposure tool downtime after cell clears
	SD_BeamRecharge	Beam recharge, recorded as exposure tool downtime after exposure tool clears
	SD_RingPM	Ring PM, recorded as exposure tool downtime after exposure tool clears
Engineering	Engineering	Cell employed in engineering activities and not available for production.
Standby/Idle	StandbyIdle_Starved	Exposure tool empty and idle while awaiting wafer from pre-exposure track (exposure tool starved from upstream)
	StandbyIdle_Block	Exposure tool loaded but idle while awaiting to unload to post-exposure track (exposure tool blocked from downstream)
	StandbyIdle_SAW	Exposure tool empty and idle during processing/inspection of SAW at any other module
Productive	Productive	Exposure tool busy during load, global alignment, step, dose control, and unload of normal wafer
	Productive_SAW	Exposure tool busy during load, global alignment, step, dose control, and unload of SAW

7.2 Unscheduled Downtimes

A fundamental experimental assumption is that the synchrotron ring and associated subsystems do not experiences significant unscheduled downtime. While the simulation is fully capable of implementing unscheduled downtime for the ring, experiments have not been executed under this experimental frame.

This assumption clearly is unrealistic, but is motivated by the lack of credible data on the reliability of synchrotron rings and peripherals operating in a production environment. While data from ALF suggest that ring availability of as much as 98% can be achieved, these field data are based on low-volume specialty production. The ALF ring historically is operated on a three-day-per-week production schedule, with the remainder of the week devoted to non-production activities appropriate to a research installation.

It is assumed that cells do not fail while inactive during scheduled downtimes, or at least that such a failure is not detected until the cell returns to an uptime state. Failures on the unit cell resulting in unscheduled downtimes are assumed to be randomly distributed according to an exponential distribution with MTBF=19,500 min (325 hrs). This failure rate is the compound result of exposure-tool failures and track failures. Exposure-tool failures represent 60.6% of all cell failures and track failures represent 39.4% of all cell failures. Recovery times after exposure-tool failures are assumed to be randomly distributed according to an exponential distribution with MTTR=240 min (4 hrs). Recovery times after track failures are assumed to be randomly distributed according to a continuous uniform distribution on the range 30 min (0.5 hrs) to 150 min (2.5 hrs).

All unscheduled downtimes for the critical lithography cells are modeled logically (but not parametrically) as failures at the exposure tool. Immediately after failure, all wafers on the pre-exposure track and on the exposure tool are sent to rework area for that cell. Wafers on post-exposure track continue processing. This assumption is motivated by modeling convenience and should reasonably capture average behavior over large numbers of failures.

8 SIMULATION EXPERIMENTS

Six simulation experiments were completed according to the experiment design summarized in Table 2. For each of the experiments, data are gathered for 52 replications, each replication simulating one-week (10080 min) of continuous (24 hrs/day, 7 days/wk) operation. Statistical counters are reset to zero between replications, while the system image is retained. The effect is to generate a single sample path simulating the continuous operation of the X-ray lithography area for a one-year period, with the output aggregated into 52 one-week batches. Each observation therefore represents a one-week count or average, and the complete sample for each output consists of 52 such observations. The use of weekly observations coincides with many of the standard performance metrics commonly understood within the industry, for example, the use of wafer-starts-per-week as a measure of fab capacity.

The use of weekly observational batches also has sound implications for the statistical analysis of the simulation output data. First, the run length of 10080 min is large compared with maximum module processing times (approximately 5.1 min), the maximum cycle-time per wafer (approximately 20 min uninterrupted), the maximum cycle-time per cassette (approximately 62 min uninterrupted), and even the maximum cycle-time per cassette train (approximately 580 min uninterrupted). This is important because the system image is not reset between runs and the initial conditions for each replication (except the first) are identically the terminating conditions for the preceding run. By design, therefore, the end of each weekly sequence is correlated with the beginning of the next weekly sequence. Given the one-week duration of each simulation run, however, the effect of such correlation on batch counts and averages is insignificant. For statistical analyses, weekly observations of each output safely can be treated as independent and identically distributed.

Second, the weekly data typically span 6 complete cell-PM downtime sequences, 27 complete beam-recharge downtime sequences, and one complete ring PM sequence. The low variability in the occurrence and duration of these events from one weekly cycle to the next implies a correspondingly low variability in the output observations.

Table 2: Summary of the Experiment Design Applied in the Simulation Study.

Experiment name	Wafer diameter [mm]	Wafers/ cassette	Field size [mm]	Exposure time/ wafer [sec]	Chips/ wafer
25_101	200	25	25x25	101	37
25_117	200	25	11x22	117	100
25_154	200	25	13x22	154	84
12_168	300	12	25x25	168	89
12_205	300	12	11x22	205	246
12_306	300	12	13x22	306	206

While unscheduled downtimes are considerably more variable (and should account for the majority of the variability in the results as a whole), the net effect should result in output estimates for one-year with excellent statistical precision. These same factors combine to imply that initialization effects should not result in biased output statistics.

Each of the simulation runs has the potential for generating copious amounts of output data. While these data are useful for model verification and validation, only key measures of system performance are collected for production runs, summarized, and reported here. These measures include wafer throughput and equipment state frequencies. Throughput is a measure of the effectiveness of X-ray lithography for volume production. For a given level of throughput, equipment-state frequencies indicate the efficiency of X-ray lithography, by accounting for the utilization of the most costly element in the tool set. For each experiment, statistics reported are the grand average, 95% t-confidence interval, minimum value, maximum value, and number of observations for the sample of weekly counts and frequencies. For each replication within an experiment, further details of individual observations also are reported for that run.

9 RESULTS AND DISCUSSION

Figure 3 is a box plot comparing wafer production results for the six experiments. In the figure, the vertical lines represent the 52-week range of the weekly observations of wafer throughput for each experiment. The box represents the 95% confidence interval centered on the mean. As anticipated, wafer throughput decreases as the size of the fields shrink, because of the increased time required to expose the increased number of fields on each wafer. Also as anticipated, wafer throughput decreases as the diameter of the wafer increases, for the same reason.

Figure 4 is a box plot comparing chip production results for the six experiments. For both 200mm and 300mm wafers, the greater number of chips on wafers with 11x22 fields results in the greatest throughput. For 300mm wafers, the larger surface area (accommodating a larger number of fields per wafer) more than compensates for the overall reduction in wafer throughput resulting from increased exposure times. Assuming comparable fabrication and wafer-sort yields, the combined effect gives a marked advantage in chip throughput for the production of 300mm wafers with 11x22mm fields.

The stacked bar chart in Figure 5 compares the frequency distribution of equipment states for the six experiments. These frequency distributions exhibit remarkably small differences across the full range of assumptions. As can be seen in Figures 6-10, there appears to be little or no statistical difference in downtimes or engineering time among the experiments. This is anticipated, since the process models controlling these states are identical in every case.

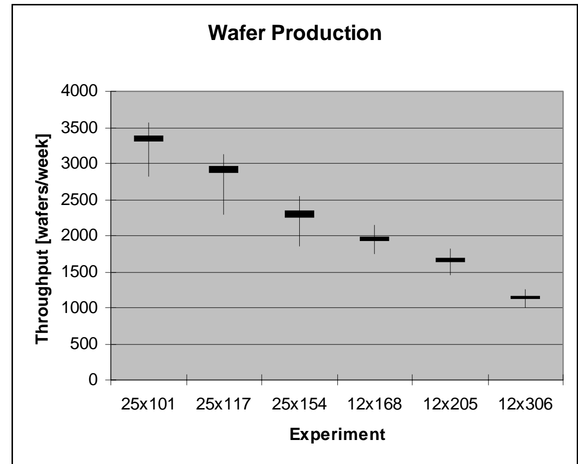

Figure 3: Comparison of Weekly Wafer Throughput

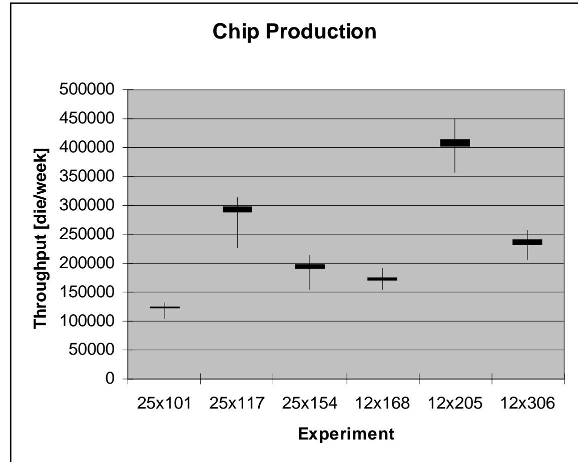

Figure 4: Comparison of Chip Throughput

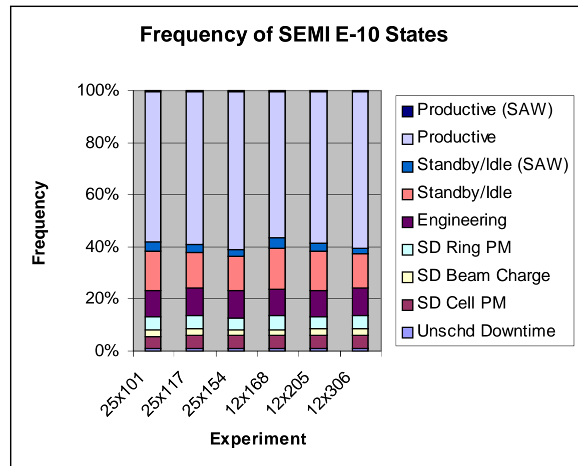

Figure 5: Comparison of Equipment States

The small differences that do appear result for the most part from the impact of event timing under the priority scheme used to account for multiple simultaneous states. This is most obvious in the scheduled-downtime state associated with ring PM as seen in Figure 9. In the third (25_154) and fifth (12_205) experiments, ring PM was initiated in one or more weeks at the same time the cell experiencing a lengthy unscheduled downtime. Since the overlapping time is charged to the failure state alone, the duration of the recorded ring-PM state was unusually small. Even where statistically significant, however, the comparisons suggest only minor differences among the estimates and static computations.

Figures 11-14 provide a closer look at the modest, but consistent and significant, differences in the tradeoff between productive time and standby/idle time. For both 200mm and 300mm wafers, productive time increases and standby/idle time decreases as the size of the fields shrink. This is attributable to the increased exposure time required for individual wafers. As the exposure time of each wafer increases, clearly the cycle time of a cassette train also increases. All else being equal, however, the *proportion* of cycle time during which the exposure tool is busy also increases.

With the number of cassettes in a train unchanged, the impact of a required reduction in the number of wafers per cassette from 25 for 200mm wafers, to 12 for 300mm wafers, more than doubles the number of setups required per wafer. As can be seen in Figures 11-14, however, the real increase in time required to process send-ahead wafers is small. Again, the increased exposure time for 300mm wafers explains this result. Because wafer throughput is almost halved (see Figure 3), the number of set-ups required per week is almost unchanged.

10 CONCLUSIONS

This paper has discussed the development and initial application a simulation model that represents the detailed logic for wafers processing through an advanced X-ray lithography cell, as well as the disturbances that interrupt processing. Under the critical assumption that no cell is ever starved for input, this unit cell model is easily scalable to represent an arbitrary number of synchrotron rings and associated X-ray lithography cells.

X-ray was selected because it is the only NGL technology with production experience. Proof the simulation concept permits operational evaluation of all the NGL technologies, so a comparative analysis can be made with existing optical equipment. This model also is easily modified to conventional-optical and alternative next-generation lithography technologies.

Performance measures that can be estimated from the simulation include the weekly wafer throughput for each cell and the frequency of equipment states for the corresponding exposure tool. Equipment states defined in the model are based on an expansion of the SEMI E-10 guidelines. This expansion explicitly accounts for downtimes associated with beam charge, cell preventive maintenance, and ring preventive maintenance, as well as for standby/idle times associated with processing send-ahead wafers and with operating conditions that starve or block the exposure tool.

The simulation experiments reported provide insight on design and operation of the lithography area. Results

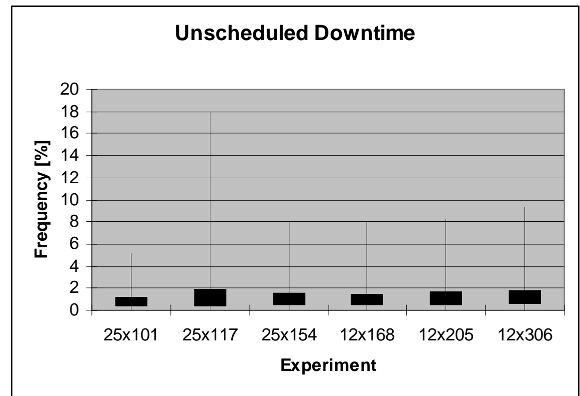

Figure 6: Comparison of Unscheduled Downtimes

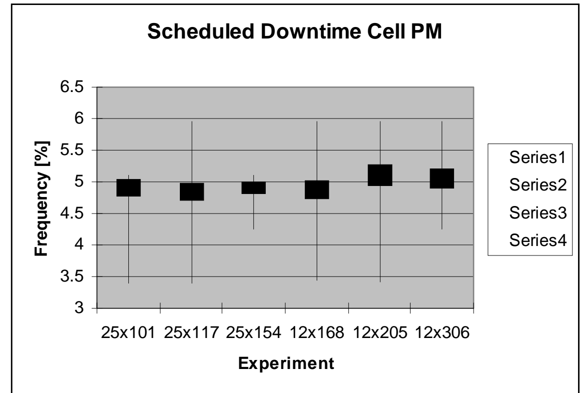

Figure 7: Comparison of Cell PM Downtimes

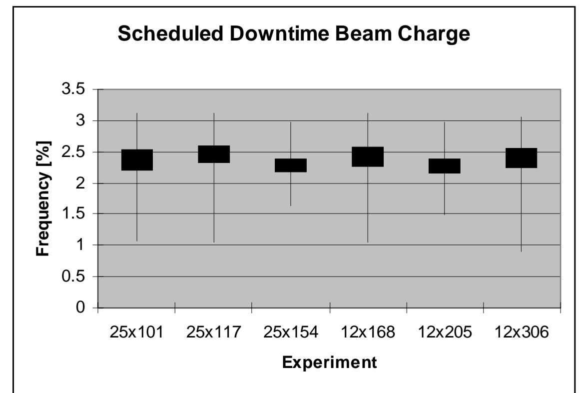

Figure 8: Comparison of Beam Charge Downtimes

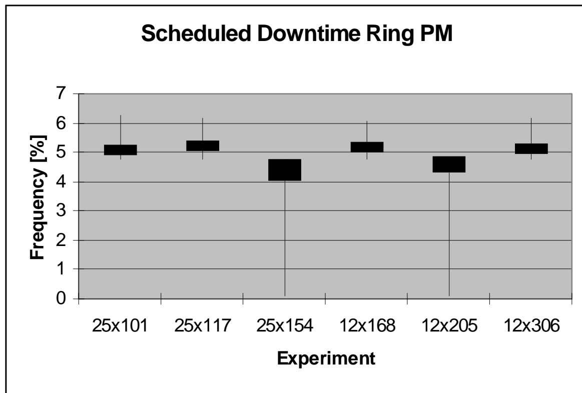

Figure 9: Comparison of Ring PM Downtimes

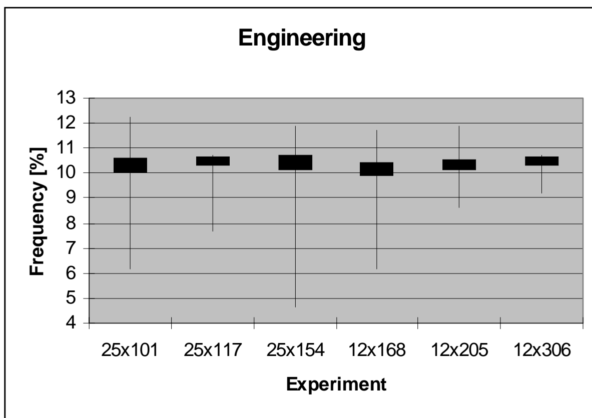

Figure 10: Comparison Engineering Times

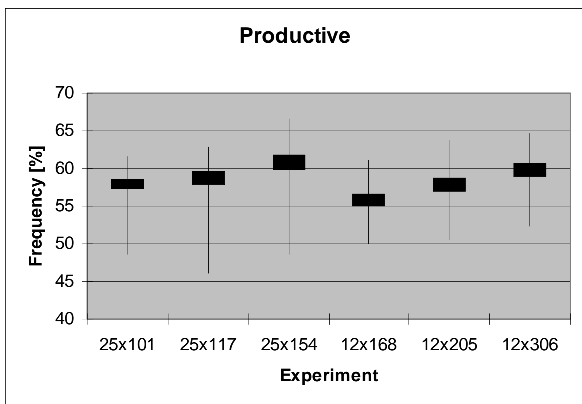

Figure 11: Comparison of Productive State

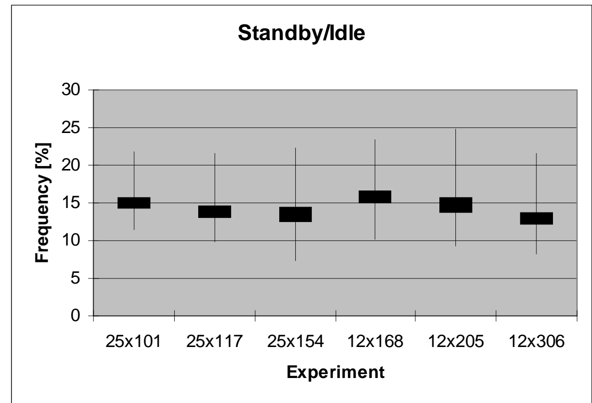

Figure 12: Comparison of Standby/Idle State

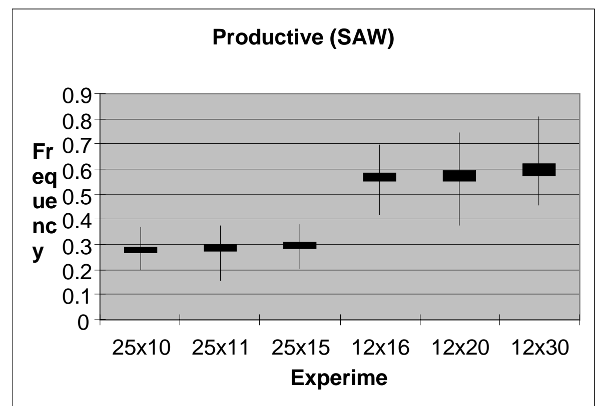

Figure 13: Comparison Of Productive (SAW) State

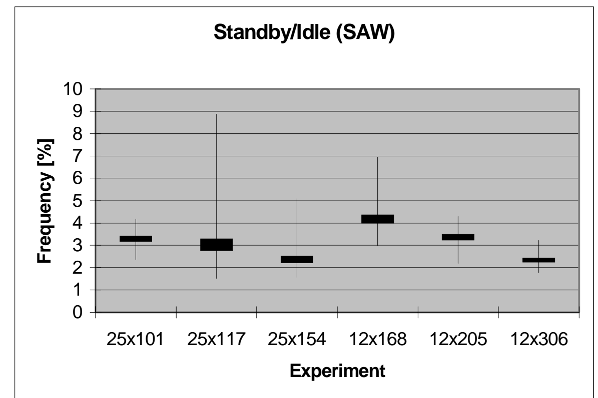

Figure 14: Comparison of Standby/Idle (SAW) State

show both obvious and subtle interdependencies of wafer throughput, chip production, tool utilization, train length, wafer diameter, and field and chip sizes. Best indications are that the move to 300mm wafers is warranted by increased productivity, assuming comparable fabrication and wafer-sort yields can be established.

The required analysis tools and modeling perspectives are now in place to address the key remaining operational issues. A first concern is the interaction of the X-ray complicated reentrant flows. This issue has been resolved in the current simulation experiments by assuming that a fab is operated such that there is always WIP waiting to be processed at the critical lithography tools. While this assumption appears to be consistent with the economic operation of an advanced wafer fab, the feasibility and implications of this assumption should be explored.

A second concern is the reliability of the synchrotron rings and the impact of unscheduled ring downtime on

production efficiency and effectiveness. This issue has been resolved temporarily by assuming that neither of the synchrotrons experiences significant unscheduled downtime. This assumption is unrealistic, but is motivated by the lack of credible data pertaining to the reliability of rings and peripherals operating in a production environment. While the simulation is easily capable of implementing unscheduled downtime for the ring, sensitivity studies remain to be executed and the best data available needs to be acquired and applied.

A final concern addresses the details of the X-ray lithography area design layout. Key issues include and transport and handling of wafers within the area and, especially, the spatial relationships between multiple cells on a common ring. Crowding between and cells is likely to create significant obstacles for operational and maintenance.

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AUTHOR BIOGRAPHIES

K. PRESTON WHITE, JR., is an Associate Professor at the University of Virginia and represents IEEE/SMC on the Board of the Winter Simulation Conference. His biography appears elsewhere in these *Proceedings*.

WALTER J. TRYBULA is a Project Manager in International SEMATECH's Advanced Lithography Thrust, with the responsibility for projects directed at producing information for narrowing the options for next generation lithography (NGL) semiconductor technology. His primary projects are focused on the evaluation of mask stability and costs for NGL. He is also exploring information-gathering technologies for bibliographically unrelated but complementary technologies. He joined SEMATECH in 1993 as a Project Manager for Simulation and Modeling with responsibility for cost and flow analyses of equipment and facilities. Prior to joining Lithography in early 1996, he was the Acting Manager of the Operational Modeling Department. His experience covers all aspects of electronics manufacturing, specializing in manufacturing productivity analysis, costing, and facility modeling. Dr. Trybula is a Fellow of the IEEE and editor of the *IEEE Transactions on Electronics Packaging Manufacturing.*