Proceedings of the 1996 Winter Simulation Conference
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AN INVESTIGATION OF OPERATING METHODS FOR 0.25 MICRON SEMICONDUCTOR MANUFACTURING

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ABSTRACT

This study investigates a number of operational issues associated with the control of microprocessor fabrication facilities, specifically expanding the domain of previous research to investigate the effects of lot size, test wafer proportion, and tool productivity on wafer fabrication performance. Response variables included cost and production performance metrics.

1. INTRODUCTION

The elements required to support and plan for a semiconductor production facility (fab) process technology and tool set is naturally partitioned into two distinct and yet interrelated groups. The first, termed *factory architecture*, encompasses strategic and technical decisions made concerning the manner in which the fab accommodates and enables operation of the process tool set. Factory architecture elements include: shell structure, tool layout, air handling, material handling and movement, fluid distribution, and tool accommodation systems.

Temporally, factory architecture issues dominate in the initial facility planning stages through tool set installation and product qualification, after which the facility infrastructure is typically set. With a typical shell design life of 10 to 15 years (Burnett 1995), the factory architecture decision making must anticipate the needs of a variety of tool sets and process technologies. This requires a degree of flexibility and robustness in all architectural decisions associated with facility design. Further, although the facility has become a shrinking portion of the overall cost of a fab, an ineffectual design (i.e., one that does not anticipate tool and process requirements and is not well integrated with operational business practices) will severely limit the long-term profitability of the business.

The second group of elements, *factory operations*, refers to the business practices that govern the operation and control of daily life within the fab. Factory operations include items such as production planning and shop floor control, yield management, staffing and training polices, modeling and simulation, decision support systems, and equipment and process control. These operational decisions dominate from the time of tool installation and product qualification throughout the active life of the fab until refit or shut down. Operational business practices are critical in the context of the evaluation and selection of factory architectural elements since the operational practices determine to what extent the potential of the factory architecture, to enable the tool set and process technology, will be realized in production.

This study reports the results of a full factorial simulation experiment (27 experimental treatments) which investigating the effects of the following operational factors: **lot size**, **test wafer level**, and **tool productivity**. The lot size factor was investigated at three levels, i.e., 12, 24, and 48 wafers per lot. Test wafers were run as a non-revenue producing product consuming 0%, 10%, or 20% of aggregate lot starts. Tool productivity refers to the *speed* of the process equipment as measured in wafers per hour. To obtain the tool productivity factor levels, the nominal equipment speeds were varied $\pm 10\%$.

A baseline simulation model with a 24 wafer lot size, 0% test wafers, and nominal tool productivity was developed using an equipment and product set previously defined by the SEMATECH capital productivity (CP) group (Rowe, et. al., 1995). This baseline model contained four process flows and 168 pieces of primary processing equipment. The primary performance metrics analyzed include cost/cm^2 (in the year 2001), cycle time, throughput, and overall equipment effectiveness (OEE). Statistical analyses of the results illustrated the significant impact data quality (with regard to tool productivity and test wafer requirements) can have on the ultimate cost and

performance of a fabricator. Overall, there was minimal performance difference between 24 and 48 wafer lot sizes. Statistical significance was found for all anticipated main effects. The impact of factor interactions was minimal, although their graphical examination allows considerable insight into fab system dynamics.

The life cycle of a modern semiconductor fabrication facility is one of constant flux. It is not uncommon for the volume and mix of products intended for a new fab to drastically change over the 18 to 36 month planning and construction phase. Once in production, the market-driven requirements to implement product enhancements, die area shrinks, tool upgrades, and new process technologies are constant. These requirements demand that the architecture of the fab superstructure and support systems be closely synchronized with efficient business and operating practices. This synchronization is required to support process technologies and tool sets that are routinely strained beyond their original design parameters. The SIA reiterates this message in the statement, *The semiconductor factory requires the following two levels of integration: 1) the process flow with the set of equipment and procedures that comprise the process and device technology, and 2) the various disciplines required to build and operate a successful factory.* (SIA 1994, p. 143).

2. PREVIOUS RESEARCH

Research into operational issues associated with microprocessor fabrication has traditionally received less attention than the more technical issues association with the engineering and physics of the production transformation process required to fabricate microprocessors. In the current climate of intense competitiveness, these operational issues have increased in importance. For example, recently Hung and Leachman (1996) attempted to apply both simulation and mathematical programming approaches to the production planning problem in the microprocessor fabrication environment. Earlier, a closed loop job release control system for the microprocessor fabrication environment was presented (Glassey and Resende 1988).. A much more complete review of production planning approaches applied to the microprocessor fabrication arena can be found in focussed survey papers (e.g. Uszoy, et.al. 1992).

Investigations into the nature of microprocessor fabrication range from empirical studies (e.g., of the relationship between die yield and cycle time (Cunningham and Shanthikumar 1996) to analytic studies (e.g. again, die yield verses cycle time (Wein 1992)). More and more, researchers are focusing on semiconductor scheduling issues (e.g., Glassey and Petrakian 1989, Lozinski and Glassey 1988, Lu, et. al., 1994, Wein 1988) and industry practices (Hood, et. al., 1995, Leachman 1994).

3. THE EXPERIMENTAL DESIGN

3.1. The Tool Set

Similar to the product specification, SEMATECH CP 200 mm wafer diameter, 0.25 μm critical dimension tool database was adopted for this study. The capacity balanced line for the four logic process flows contains 168 primary processing tools (see Table 1). The capacity balancing was completed to achieve 20,000 wafers starts per month with a cycle time to raw processing time ratio of less than 2.5 for a 25 wafer lot size.

The parametric tool data contained in the database are representative of the SEMATECH estimate of mature production tools purchased in 1998 and operating in 2001 (Rowe, et.al. 1995). In an effort to more accurately reflect typical (rather than best-of-breed) manufacturing operations, selective tool parameters were degraded. Reliability parameters: mean time between failure (MTBF), mean time to repair (MTTR), E10 downtime percentages, and E10 engineering time percentages from the CP 0.5 μm tool database (Elahi, 1995) were superimposed over the 0.25 μm values. Preventive maintenance times also were lengthened by 50% to dynamically model the myriad of minor productivity losses and delays routinely encountered in fab operations (Rowe, et.al. 1995, p. 13). Other tool parameters, including setup and run-out times, were unchanged.

It should also be noted that critical dimension, overlay, and patterned defect inspection tools for the lithography sector are the only metrology tools represented in this simulation model. The omission of other metrology or in-line test equipment is a significant deviation from most current leading edge semiconductor manufacturing environments and will be addressed in future studies.

3.2. The Product

Four (200 mm wafer diameter, 0.25 μm critical dimension) logic products with associated process flows as specified in the SEMATECH CP program (Rowe, et. al., 1995) were the basis for this study.

The four products included in the simulation model are as follows:

1. **High performance logic** (suitable for advanced microprocessor fabrication).
2. **Vertically modulated well** (VMW) (featuring MEV implant and shallow trench isolation).
3. **Low power logic** (based on the VMW process).
4. An **application-specific integrated circuit** (ASIC) process (no deep ultraviolet (DUV) lithography).

Throughout the discrete event simulations, each of the four products was allocated one-fourth of the available product wafer starts.

Table 1: Tool Type Summary

Process Sector	# of Tools	Tool Type	# of Tools
Litho-graphy	36	DUV Litho (248nm)	5
		0.35μ I-Line	6
		Large Field I-Line	7
		Litho Apply	2
		CD Measure	7
		Overlay	9
CFM	3	Defect Inspection	3
Etch	24	Oxide/Nitride Etch	8
		Metal Etch	5
		Poly/Si Etch	3
		CDE	2
		W Plug Etch	3
		Oxide Etch	3
Surface Preparation	19	Vapor Pre Clean	1
		Critical Pre Clean	3
		CMP Post Clean	3
		Std Wet Clean	12
Thermal	29	LPCVD Deposition	9
		Ox and Anneal	14
		RTP	6
Implant	7	Hi-I Implant	2
		Med-I Implant	4
		MEV Implant	1
BEOL Films	44	Asher	16
		APCVD BPSG	1
		CAP Oxide	4
		PECVD	1
		Ti, TiN Deposition	5
		Sputter TACS	5
		W CVD	2
		CMP Oxide	6
		ILD Gap Fill	4
Misc	6	Parametric Tester	3
		Backside Grind	2
		Laser Scribe	1
Total	**168**		**168**

An additional product, i.e., test wafers, was also included in our model. The test wafer product followed the high performance logic process flow. The only deviation from the SEMATECH specification of process flows was the slight adjustment of processing times required for variations in the lot size, and the inclusion of material movement times. The lot size modification was instituted to facilitate the inclusion of lot size as an experimental factor. The addition of material movement times created new steps in the flows but had no effect on existing ones.

3.3. Simulation Model Details

The fab layout was developed based on the CP Rev. 2 data set, resulting in model requiring 51,905 ft^2 of primary cleanroom space.

3.4. Experimental Factors

The experimental factors of lot size, tool productivity, and test wafers are discussed below. A brief description of the supplemental factors, WIP, and material movement time also is included.

Lot Size: Lot size was examined at three levels: 12, 24, and 48 wafers per lot. It was assumed that process and transfer lot sizes are equal. The lot sizes of 24 and 48 wafers were selected to reflect the lot sizes of existing fabs. A lot size of 12 was investigated as one that may be of interest for future fabs that produce a wide variety of low volume products. Twelve wafer lots are also of particular interest for proposed 300 mm fabs.

A primary objective in the development of the fab layout model was to minimize product travel while maintaining proper relative location of tools. To minimize product travel between tools, the process flow was analyzed to determine which tools should be in close proximity to one another. Tools that are expected to remain in the fab for a long period of time were located near the center of the fab, and tools required more frequent repair, upgrading, or modification were placed on the periphery. After determining tool location within the bays, the optimal arrangement of the bays was determined.

The tool layout was generally in a format known as a farm arrangement, i.e., with homogeneous tools grouped together. In only a few instances, such as ashers, were homogeneous tool types dispersed throughout the fab. The latter method was chosen for this study to simplify the calculation of process times where both lot size and tool productivity required modification.

Tool Productivity: The three tool productivity factor levels were coded as **low**, **nominal**, and **high**. The central level, nominal, represents the tool productivity (or speed of the tool), measured in wafers per hour. The low level corresponds to slowing down the productivity of each tool in the line by 10 %. This was achieved by multiplying the tool process times by 1.1. Likewise, the high level of tool productivity corresponds to speeding up the tools by 10%, as measured in wafers per hour. This level was implemented by multiplying the process times by 0.9. This treatment was similar for both serial and batch tools.

The wafers per hour used in the nominal level of tool productivity represents a consensus between IC manufac-

turers and equipment suppliers, as documented by the SEMATECH CP program. The productivity consensus is meant to be indicative of best-of-breed tools purchased in the 1998 time frame. The 10% variation in tool *speed* to achieve the high and low factor levels were chosen to illustrate the impact of deviations from intended wafer per hour productivity rates. This situation is one that may arise when wafer per hour rates realized on tools in production do not correspond to the rates assumed when the original capacity and space planning was completed for the fab. Such *speed* differences may arise for several reasons: tool suppliers may not be selected when the facility is designed, tools may not perform as advertised, final tool selection may be based on criteria other than throughput, or tools may be required to run processes that differ substantially from those anticipated at the time of facility design.

Test Wafers: Test wafers were examined at three levels: **0%**, **10%**, and **20%** of total wafer starts. Uniform terminology regarding test, monitor, control, non-prime, and non-product wafers often is not used. In this paper, *test wafer* is assumed to include the preponderance of non-product wafers that must be started in the line, regardless of wafer ultimate conditions of usage. This definition is intended to be similar to the SIA roadmap usage of *monitor wafers*, which refers to desired ratios between product and total wafer starts/usage [SIA 1994, p.164].

There are several ways to model test wafers. In reality, test wafers require a wide variety of films and structures to fulfill their myriad functions. An accurate portrayal of test wafers was beyond the scope of this project. However, the most important factors to consider for test wafers are their impact on the cost of silicon purchased, and the capacity loss of tools required to process and run the test wafers. For this study, test wafer costs were incurred as a percentage of total product wafer starts. The concept of test wafers as a capacity loss on the tool set was also included.

This capacity loss was implemented by the creation of a fifth product type: test wafers. The test wafer product followed the same process flow as the high performance logic. The number of test wafer starts per month was calibrated to the total 20K per month of releases. The other four product types were adjusted to maintain an equal 25% mix for the remainder of the available monthly wafer starts.

The 0% level was chosen to represent the optimal potential of the system as well as to allow easy comparison to other studies that do not consider test wafers as a capacity loss. Ten percent was considered to represent best-of-breed operations for fabricators in 1995 and the Roadmap goal for 1998. Finally, 20% was selected as representative of the 1995 Roadmap goal [SIA 1994, p.164] and perhaps more typical current fab operations.

3.5. Supplemental Factors

Follow-up experimentation was conducted including various level of shop work-in-process (WIP) levels and various levels of transport time associated with the automated material handling system (AMHS). For a complete discussion of the results of the follow-up experimentation see Hallas, et. al., (1996).

3.6. Metrics

Four metrics were collected in this study:

- cost per square centimeter of silicon produced in the year 2001 (cost/cm^2),
- throughput,
- cycle time, and
- OEE.

The first three measures represent three of the five defined factory integration performance metrics itemized in the Roadmap [SIA 1995]. The other two SIA-listed metrics, yield learning curve and extendibility, both require an extended temporal analysis of a fab life cycle that was beyond the scope of this effort. The last primary metric, aggregate OEE, is reported for each experimental treatment. While OEE is typically a tool-based measure (Ames, et. al., 1995, Barber 1995), it is reported here as an aggregate line measure.

A full factorial experiment was conducted (3^3) on the primary experimental factors. Discrete even simulation was in conjunction with static cost calculations to model fab performance. Ten batch means (replications) of one year were analyzed, with the initial transient data (one year) discarded. Randomly selected initial seeds for the simulator random number generators were selected to support the observation independence assumptions associated with analysis of variance.

4. ANALYSIS OF RESULTS

Cost $/cm^2 SI: For cost, as well as other response variables, there was little impact on the system between 24 and 48 wafer lots (See Figure 1).

This is, to some degree, due to the fact that the line balancing was done using a 25 wafer lot size. However, it is not clear that rebalancing the line would substantially improve efficiencies for 48 wafer lots. Further, the 12 wafer lot size incurred a large setup penalty. This relationship between the different lot sizes appears to be due primarily to the shifting bottlenecks that result from the unbalanced lines. Since 24 and 48 wafer lots share nearly the same setup-independent bottlenecks, there is

little performance difference between these two lot sizes. Because the 12 wafer lot models have a setup-dependent bottleneck, there is a significantly greater cost for its use.

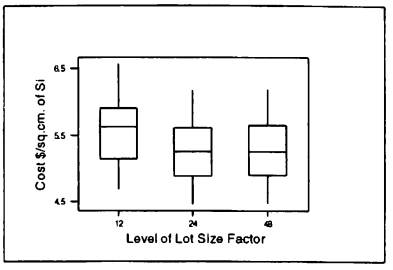

Figure 1: Lot Size Factor Effect on Cost $/cm^2 SI

Alternatively, increasing tool productivity through all levels has a positive impact on cost from the increased throughput it allows (See Figure 2).

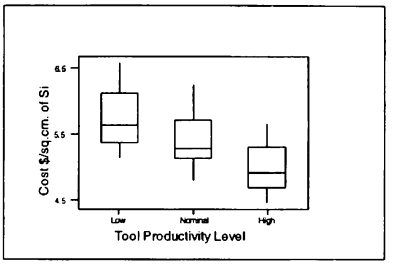

Figure 2: Tool Productivity Effect on Cost $/cm^2 SI

Increasing test wafers negatively influences cost by using more production capacity for non-revenue producing wafers. (See Figure 3). As indicated in Table 2, all three factors are significant.

The statistical significance of the interactions may be, to some degree, due to the extremely long simulation runs which allow for very small within-group variation. Therefore, although most interactions are statistically significant, a focus on the statistically significant main effects may be appropriate.

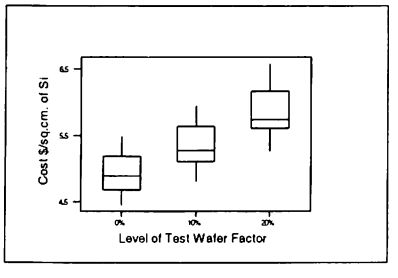

Figure 3: Test Wafer Effect on Cost $/cm^2 SI

Table 2: ANOVA Results for Cost $/cm^2 SI

Cost $/cm^2 SI			
Source	**df**	**F**	**p-value**
Lot Size (LS)	2	1066.77	4.7×10^{-121}
Tool Productivity (TP)	2	4927.56	2.2×10^{-197}
Test Wafer (TW)	2	7353.79	4.3×10^{-218}
LS×TP	4	16.00	1.2×10^{-11}
LS×TW	4	24.62	4.02×10^{-17}
TP×TW	4	23.78	1.3×10^{-16}
LS×TP×TW	8	1.18	0.3202

Throughput: Throughput of the simulated fab was measured in terms of wafers produced per week. All three factors show a substantial statistical impact on throughput (See Table 3).

Table 3: ANOVA Results for Throughput

Throughput			
Source	**df**	**F**	**p-value**
Lot Size (LS)	2	1980.45	3.8×10^{-151}
Tool Productivity (TP)	2	$1.0\times10^{+4}$	4.4×10^{-234}
Test Wafer (TW)	2	$1.5\times10^{+4}$	2.9×10^{-255}
LS×TP	4	33.24	4.12×10^{-22}
LS×TW	4	2.66	0.033405
TP×TW	4	47.08	2.86×10^{-29}
LS×TP×TW	8	1.99	0.0483

Again, although the interaction effects are statistically significant, they explain much less of the variation than the main effects and are well behaved when plotted. As expected, throughput increases as tool productivity increases (See Figure 4).

Additionally, throughput decreased significantly as the number of test wafers increased (see Figure 5). When modeled as a direct incursion on capacity, the stark impact of the level of test wafers, a factor largely under engineering control, is clear.

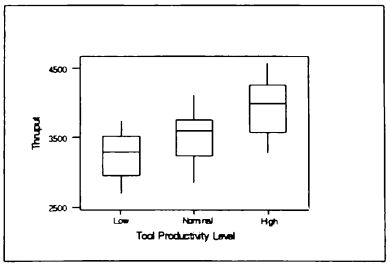

Figure 4: Tool Productivity Effect on Throughput

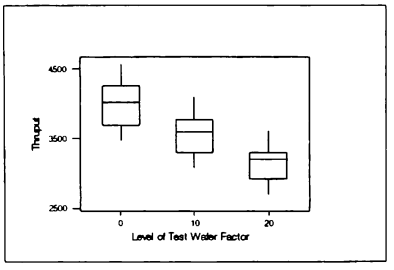

Figure 5: Test Wafer Effect on Throughput

Similar to the cost main effects, increasing from a lot size of 24 to 48 provides no significant benefit in throughput. In fact, in Figure 6 the impact is slightly negative.

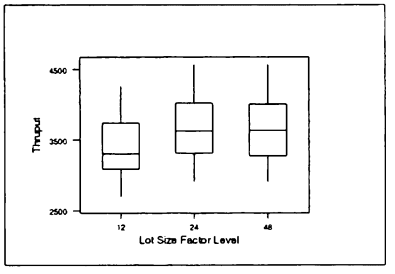

Figure 6: Lot Size Effect on Throughput

Much of the throughput loss seen in the 12 wafer lot size is explainable through the treatment of setups. This is discussed further in the cycle time section below. As expected, the throughput main effects are inverted relative to those of the previous metric, cost.

Cycle Time: Cycle time of the simulated fab was measurd in terms of hours. The percentage of test wafers had no impact on the cycle time of the four process flows (see Table 4).

This result can be seen by the small F value for test wafers and is logical due to test wafers following the same process flow as high performance logic. Otherwise, lot size (Figure 7) and tool productivity (Figure 8) trends follow that of cost and are inverted relative to throughput.

An examination of the 12 wafer lot size treatments will show that cost and cycle time increase while throughput and OEE (discussed later) decrease relative to treatments with 24 wafer lots.

The only counterintuitive result here is the cycle time seems to increase slightly when lot size changes from 24 to 48. This occurs due to the conservative setup assumptions used for this study. There are natural penalties that a small lot size would incur, such as more frequent sequence dependent setups due to increased switching between product and recipe queues, longer batching delays, and more congestion due to a higher number of lots in the line. However, in this study the 12 wafer lot size incurred further inefficiencies because only process times, and not setups, were modified for lot size changes. The setup frequency for some tools in lithography, CMP, and RTP have setups based on the number of lots processed. Therefore, treatments with 12 wafer lots incurred substantially more setups per wafer than 24 wafer lots (while 48 wafer lots received less). This is the cause of the observed cycle time increase for the 12 wafer lots.

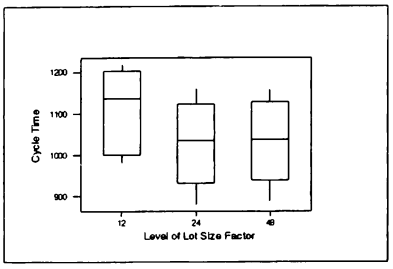

Figure 7: Lot Size Effect on Cycle Time

Table 4: ANOVA Results for Cycle Time

Cycle Time			
Source	**df**	**F**	**p-value**
Lot Size (LS)	2	1607.15	7.8×10^{-141}
Tool Productivity (TP)	2	8019.51	4.6×10^{-233}
Test Wafer (TW)	2	0.30	0.741092
LS×TP	4	21.01	6.8×10^{-15}
LS×TW	4	4.81	0.000945
TP×TW	4	0.82	0.513472
LS×TP×TW	8	0.96	0.467984

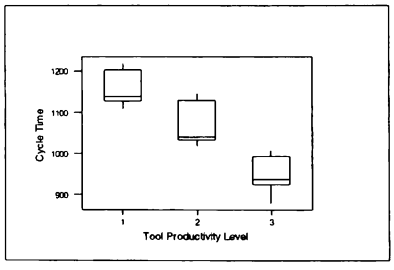

Figure 8: Tool Productivity Effect on Cycle Time

Although in many cases, significant interactions cause one to doubt the assessment of the signifiance of main effects, in this instance, the assessment of the significance of the test wafer factor seems appropriate.

OEE: OEE measures the amount of tool potential that is realized in production. Table 5 indicates significance of all main and interactive effects of this experiment. Alternatively, since tool productivity essentially alters the denominator for OEE (i.e., the anticipated potential of tools), it is practically unaffected by tool productivity, as can be seen on the main effects graph (see Figure 9).

Table 5: ANOVA Results for OEE

OEE			
Source	**df**	**F**	**p-value**
Lot Size (LS)	2	3134.29	3.1×10^{-174}
Tool Productivity (TP)	2	117.64	1.86×10^{-36}
Test Wafer (TW)	2	2.3×10^{-4}	1.1×10^{-277}
LS×TP	4	36.79	4.85×10^{-24}
LS×TW	4	12.26	4.27×10^{-9}
TP×TW	4	3.81	0.005041
LS×TP×TW	8	2.99	0.003247

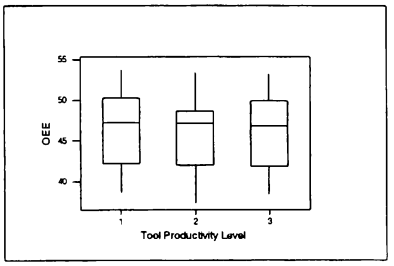

Figure 9: Tool Productivity Effect on OEE

In other words, changing the productivity (or speed) of a particular tool has little practical effect on its utilization and thus its OEE. This observation reiterates the need to ensure that a macroscopic view of the system is taken at all times to avoid myopic efforts at productivity improvement. Thus, although tool productivity is statistically significant in the model, the variation it explains is an order of magnitude less than the factors of lot size and test wafer percentage. Again, this statistical result may arises because of the cohesive simulation data provided by the extreme length of the replications.

Other than with the results associated with tool productivity, OEE results generally mimic those of throughput and follow the inverse of cost and cycle time (see Figures 10 and 11).

5. CONCLUSIONS AND EXTENSIONS

In general, results indicate minimal differences in performance between 24 and 48 wafer lot sizes, with significant differences in performance at 12 wafer lot sizes. Alternatively, clearly for specific markets or market conditions, 12 wafer lots still may be the preferable alternative. The impact that tool productivity has on system performance highlights the importance of data quality during the iterative strategic planning phase of a fab. Viewing test wafers as a capacity loss (in addition to the added material and logistical costs) demonstrated the direct impact that they can have on the bottom line. Lot size, tool productivity, and test wafer percentage were not found to interact materially with respect to measures. Overall, our results indicate an extreme sensitivity of a variety of fab performance measures to constraints determined by operating characteristics, such as raw processing time and setups, was shown. The interested reader is referred to the full paper [Hallas, et. al., 1996] for additional detail and discussion.

The results of follow-up experimentation indicated that inventory (WIP) level a large impact on fab performance, with results corresponding to those anticipated by queuing theory, while material movement time had a relatively negligible impact.

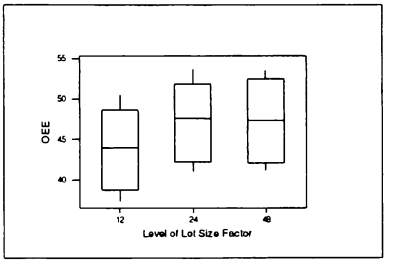

Figure 10: Lot Size Effect on OEE

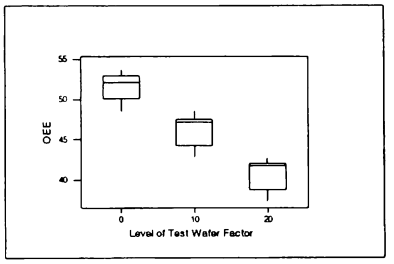

Figure 11: Test Wafer Effect on OEE

Several extensions are suggested by the results of this work. First, to provide a much needed validation, industry benchmarking analyses would be useful for comparing actual fabs with various treatments of an experimental design. Further, studies incorporating specific cost considerations in the layout design process (possibly seeking the minimum investment fabricator) would be useful. Possibly most pertinent to this study, the common practice of running various lot sizes concurrently within the fab should be investigated.

ACKNOWLEDGMENT

The authors wish to extend a special thanks to Steven Brown and Bill Jacobs for their guidance and support. In addition, we wish to thank Rick McKiddie and Scott Chandler for their technical contributions.

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