Proceedings of the 1992 Winter Simulation Conference
ed. J. J. Swain, D. Goldsman, R. C. Crain, and J. R. Wilson

MODELING THE LOT SELECTION PROCESS IN SEMICONDUCTOR PHOTOLITHOGRAPHY PROCESSING

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ABSTRACT

In this paper, we address the problem of accurately modeling the lot selection process in semiconductor wafer fabrication. We present two alternative processes for modeling the lot prioritization/selection process: prioritization before insertion in queue, and prioritization before lot selection, and discuss an implementation of the second alternative.

The implementation discussed is part of a detailed model of the photolithography process area at an AT&T Application Specific Integrated Circuit (ASIC) wafer fab. The process model will also be used in models of other fab processing areas under development.

1 INTRODUCTION

The prioritization of queued jobs (wafer lots) in integrated circuit device manufacturing is a complex process. The factors that influence lot selection are numerous, and a lot's priority as determined by these factors can change between the time it arrives in queue and the time it is selected for processing. This paper discusses the modeling of the lot selection process in a model of the photolithography process for an Application-Specific Integrated Circuit (ASIC) wafer fabrication facility.

The remainder of the paper is organized as follows: Section 2 describes briefly the photolithography manufacturing process in semiconductor fabrication, while Section 3 discusses the lot prioritization/selection decision process. Section 4 defines the alternative modeling constructs considered for modeling the lot selection process, and Section 5 describes the process as it was modeled.

2 PHOTOLITHOGRAPHY PROCESSING

In semiconductor fabrication, circuit elements are produced by the controlled introduction of impurities into selected regions of a silicon wafer (doping). Photolithography processing is used to create the patterns that will define the areas where doping will and will not take place on the wafer. The process has three primary steps [Wolf and Tauber, 1986]: First, the wafers are coated with a photosensitive resist. The wafers are then exposed to light. A pattern mask (reticle) is used to define the desired circuit feature pattern, by controlling the wafer areas in which the applied photoresist is exposed to light. Finally the wafers are sent to a developing process, where the exposed photoresist is removed. The remaining photoresist protects the wafer sections it overlays as impurities are introduced during subsequent processing, thus creating the desired circuit functionality.

Complex Very Large Scale Integration (VLSI) devices are produced by fabricating many different layers of circuit elements, and interconnecting selected elements from the different layers. This involves the sequential transfer of many different circuit feature patterns, with each new pattern transferred resulting in a new layer, or level, of circuit elements being defined on the wafer.

3 LOT PRIORITIZATION/SELECTION

There are many factors that may be considered when prioritizing lots awaiting processing in a wafer fabrication line, including product demand, lot due date, down-stream facility capacities and queue sizes, and facility maintenance schedules. We assign a processing priority to each waiting photolithography job based on the following two factors:

1. **Common Processing Requirements (Sibling Lots).** In many semiconductor fabrication processes lengthy set-up times are needed when the processing requirements for the next lot to be processed are different from those of the lot just completed. This is particularly true in photolithography for ASIC wafers, where the feature pattern being transferred to a wafer is uniquely defined by the product and the circuit element layer being produced. Each such change necessitates changing pattern reticles and verifying the alignment and focus of the new reticle. For such processes it might be efficient to run all lots needing the same reticle (Sibling Lots) before running a lot that would necessitate a reticle change.

In this discussion, we assume that there is only one copy of each reticle required for processing. Thus, if Reticle A is loaded on Photolithography System 1, then lots requiring reticle A can be processed only on System 1 until the reticle is unloaded from the system.

2. **Product Priority.** Each lot is assigned a processing priority. In this discussion, we define two priority levels: hot and regular, and assume that lot priority is function only of product-type. These assumptions are made to simplify the discussion of the lot prioritization/selection process; typically there are several different priority levels used, and priorities are assigned on a lot-by-lot, rather than a product-by-product basis. The priority assigned to a product (lot) may change during processing.

Figure 1 presents a flow chart of the evaluation process. The process is invoked each time a photolithography unit becomes available. As shown in

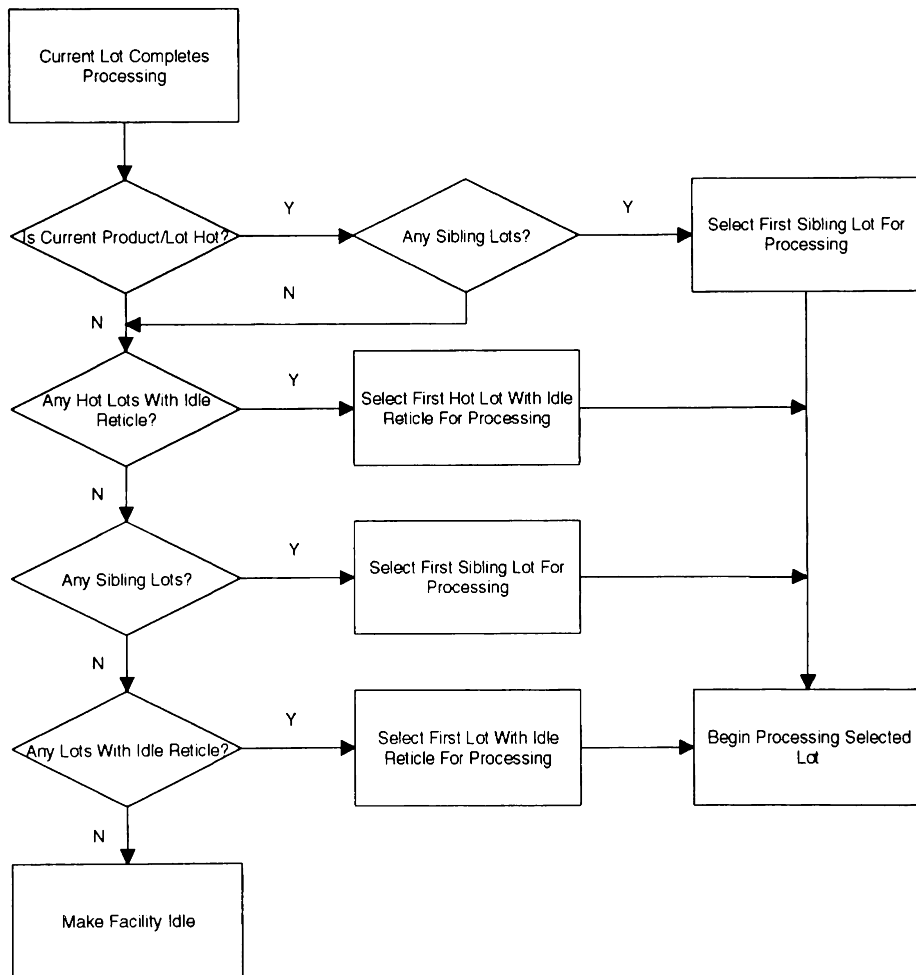

Figure 1: Lot Prioritization/Selection Process

the figure, lot priority is a function both of product priority and processing requirements. Siblings of a hot lot have highest priority on the system where their reticle is loaded, but no priority elsewhere. Hot lots whose required reticle is not loaded on another system have the next highest priority. Siblings of regular priority lots will be processed only when no hot lots are present. Regular priority lots whose required reticle is not loaded elsewhere have lowest priority.

4 ALTERNATIVES FOR MODELING THE LOT SELECTION PROCESS

The lot prioritization/selection process discussed above is implemented in a model of the photolithography area of an AT&T ASIC fab. In developing the model, which is coded in SIMAN [Pegden, et al., 1990], two approaches were considered.

4.1 Prioritize Lots As They Arrive At The Photolithography Queue - Select The First Lot In Queue When Resources Become Available.

The priority of a lot is evaluated as it arrives for photolithography processing. The lot is then placed in queue (or is placed in one of a set of queues) based on its priority. When a photolithography processing system becomes available, it is seized by the first lot in queue. There are two problems with this approach. First, it is difficult to model a lot prioritization function (to order the lots in queue) that properly reflects the relationship between lot processing priorities and sibling lot priorities shown in Figure 1. Secondly, even if such a prioritization function could be derived, we would have to create a process to reorder the queue when necessary (e.g. when a lot priority changes from regular to hot).

4.2 Lots Are Placed in Queue Based on Arrival Time (FIFO) - When Resources Become Available, Lot Priorities Are Calculated And The Lot With The Highest Priority Is Selected.

Lot processing priority is not considered until resources become available. When a resource becomes available, the evaluation process shown in Figure 1 is initiated. This models the lot selection process as it actually occurs in the wafer fab, and avoids the implementation problems associated with the approach suggested in the previous section. For these reasons, we adopted this approach to model the lot prioritization/selection process in a photolithography processing model. The details of implementing this approach are discussed in the next section.

5 A MODEL OF THE LOT SELECTION PROCESS IN PHOTOLITHOGRAPHY PROCESSING

The lot prioritization process described in Section 4.2 is modeled using standard constructs available in the SIMAN modeling language [Pegden, et al., 1990]. In Section 5.1 we discuss the lot prioritization model. In Section 5.2 we discuss two issues that arose during verification of the model.

5.1 The Basic Process Model

Lots arriving for photolithography processing are placed in a single, detached queue (the PHOTO_GROUP_QUEUE). There are three attributes associated with each lot:

1. Product-type.

2. Photo mask level. Photo mask level corresponds to the level of the circuit feature pattern that is being transferred onto the wafer substrate; product-type and photo level uniquely determine the reticle required by the lot during photo processing.

3. A flag indicating whether this lot is the first lot of its job-type currently in the system. Job-type is defined by product-type and photo mask level. If the lot has sibling lots ahead of it in queue or if there is a sibling lot already in process, then this flag is set to OFF. If the lot finds no sibling lots in the system when it arrives, then this flag is set to ON.

When a photolithography processing system is about to become available (i.e., the lot that has seized the processing system has completed its processing delay but has not released the resource) the prioritization process begins. The current lot (the entity that is about to release the system) searches the PHOTO_GROUP_QUEUE (using the SIMAN SEARCH block) for the first lot that satisfies the following two conditions:

1. The lot must meet the criterion being evaluated. If the product-type priority of the current lot is HOT, then a search is made for

sibling lots. If no sibling lots are found, or if the product-type priority is not HOT, then the model searches for lots with priority equal to HOT. If no HOT lots are found (and if the product-type priority of the current lot is not HOT), then a search is made for the sibling lots. Finally, if the previous searches are unsuccessful, then any lots in queue are considered. And,

2. All resources required to process the lot must be available. Because a product lot is not removed from the PHOTO_GROUP_QUEUE until it has been selected for processing, the entity that removes it from the queue must ensure that all required processing resources are available as a condition of selection. Required resources are a photolithography processing system and the mask reticle associated with the lot's product-type and photo-level. In this model there is exactly one reticle for each photo-level of each product.

Because the next lot to be processed on a given photolithography system is selected only by the lot currently controlling that system, system availability is assured. Similarly, if the lot currently controlling the system selects a sibling lot to be processed next, then the availability of required reticle is assured. If the lot selected is not a sibling of the lot currently in process, then it will be a first-of-its-job-type lot (among sibling lots, lots are selected for processing on a FIFO basis). It this case too, reticle availability is assured. The reticle required by a first-of-its-job-type lot must have been idle when that lot entered the system (the lot had no siblings in process when it arrived).

The selected lot is removed from the detached queue (using the SIMAN REMOVE block) and allowed to SEIZE the photolithography processing resource just released by the lot doing the selecting. If no lot is selected the processing resource enters an idle state.

5.2 Modeling Issues

5.2.1 Recovery From Processing System Idle States

In the basic system proposed above, the lot selection process occurs while, and only while, the resource for which a lot is being selected is still busy. If the resource enters a idle state, the current-job-selects-next-job loop is broken. This problem was corrected by created a special entity to jump-start idle processing systems. If a product lot is the first of its job-type, it checks the status of the processing systems before entering the PHOTO_GROUP_QUEUE. If an idle system is detected, the lot issues a jump-start request. The jump-start entity then acts as if it had just completed processing on the idle system, and enters the selection process.

5.2.2 The Possibility Of Multiple Selections For One System

The timing of events during the selection process is critical. Any non-zero delay between the time the current lot releases its resource and the time the selected lot seizes that resource results in a non-zero probability that, through the jump-start process, two lots will be selected for a single resource. To avoid this, we modeled all process delays as occurring outside the selection process loop. Thus, the lot prioritization/selection process occurs in zero-time on the event calendar.

6 SUMMARY

In this paper, we addressed the problem of accurately modeling the lot selection process in semiconductor wafer fabrication. We described a lot prioritization process for semiconductor photolithography processing and presented two alternative approaches for modeling that process: prioritization before insertion in queue, and prioritization before lot selection. The advantages and disadvantages of each approach were discussed. Finally, an application of the second approach, prioritization before lot selection, was presented.

The application discussed is part of a detailed model of the photolithography process area at an AT&T wafer fab. The process model will also be used in models of other fab processing areas under development.

ACKNOWLEDGEMENTS

The author thanks D. Fresonke, M. Jansen, M. Mollaghasemi, J. Murray, and A. Woodard for their many helpful comments during the preparation of this manuscript.

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