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MODELING AND ANALYSIS OF A NEW PRODUCT DEVELOPMENT IN ELECTRONIC SUB-ASSEMBLY MANUFACTURING

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ABSTRACT

This paper discusses the use of simulation modeling in the analysis of a new process technology in electronic sub-assembly manufacturing to support the formulation of assembly, test, and repair strategy for volume manufacturing. The emphasis of the model is on the performance of the process from a capacity and quality standpoint. The study highlights the impact of defects (material and process) in parts per million, and manufacturing process strategy on:

- throughput,
- work in process,
- cycle time,
- process yield,
- and defect escapes.

A modular approach to simulation modeling is described. In this approach users specify the characteristics (e.g. repair time) of a particular process step at a high level within the modular code. The modular code then translates this characteristic into the simulation code needed to represent that characteristic. The modular approach allows for quick and easy model development without repetitive code writing.

1. INTRODUCTION

This paper presents a summary of a process analysis project performed as part of a new product and process development effort. This paper discusses techniques used in Digital to support decision making in a dynamic business environment.

The computer industry currently faces business pressures requiring immediate responses. The customer wants increasingly high quality and reliable systems requiring manufacturing to have greater control over its processes. Additionally, computer systems are becoming commodities requiring shorter production cycle times and lower costs. Finally, technologies are being introduced more rapidly, driving time-to-market and time- to-volume into shorter cycle requirements. All these factors require Design and Manufacturing to shorten their time for delivery of effective product and process designs and to move from the serial approach of designing and manufacturing the product to concurrent engineering of product and processes.

To concurrently engineer both product and process, it is necessary to test these designs quickly. This cannot be accomplished using physical models. It is necessary to build soft images of products and processes to test these designs. Logic system simulators have removed the necessity for breadboards and have reduced the time to deliver a defect-free product design. Additional efforts, including the approach presented in this paper, are directed toward the development of similar capabilities for process development.

Process development should be considered in two ways: 1) the capability of the process to deliver the product and 2) the ability of the process to deliver the product in a cost effective manner. The latter is the principle concern of the present analysis which provides an approach for evaluating the relationship between incoming quality levels, assembly quality levels, test screen strengths, cycle time and capital requirements. With this approach, it is possible to understand the cost relationship between test development, assembly process development and volume process costs. With this information, appropriate business decisions can be made during development concerning the investments necessary for both the development and volume cycles.

1.1 Analysis Environment

The manufacturing environment under analysis is a new process startup electronic sub-assembly line based on new leading edge technology. Electronic sub-assembly manufacturing involves the assembly and test of electronic sub-assemblies (henceforth referred to as sub-assemblies) prior to shipment to the next stage of computer manufacturing. The production goal is to ensure that the sub-assemblies yield high quality and reliability with minimum operating cost. The study supports strategy formulation for the development of assembly, test, and repair processes. The ability to evaluate the impact of different strategies ensures that optimum conditions are defined to meet the sub-assembly manufacturing goals.

Test, inspection, and repair comprise a large portion of the overall operations cost in this type of manufacturing. These costs are highly dependent upon process yields, the primary indicators of manufacturing quality. Improving the low yields which are so prevalent within leading edge technology manufacturing thus offers significant opportunities for lowering costs. Process yields can be significantly increased by controlling the level of defects received (incoming quality) and generated (process induced) and by increasing the capture rate and repair of these defects. Vendor quality levels can be evaluated and driven by analyzing the impact of incoming material quality on the process. Manufacturing test and repair strategies can be put in place to ensure process induced defects are removed. The identification and removal of defects ensure that product quality levels are maintained to support the product goals.

1.2 Analysis Objectives

Three main objectives dominate this analysis:

- To characterize, by source and cause, the defects generated by the manufacturing process.
- To develop process documentation as a communication tool between process development and manufacturing engineers.
- To determine the manufacturing volume requirements.

2. MODELING METHODOLOGY

In this section we discuss the modeling methods used to analyze the manufacturing environment. The analysis objectives are accomplished through three modeling tasks:

- To study the process from a quality standpoint by evaluating the types of incoming and process induced defects that potentially limit process yield.
- To have a conceptual representation of the process under development. The model should be sufficiently general to represent the whole process yet have enough detail to represent specific process steps. The ability to easily modify the model to keep up with the changes being made to the process is a necessity.
- To develop a dynamic simulation model that can represent the performance of the sub-assembly manufacturing process from a capacity and quality standpoint.

The dynamic model should process test results and failure data to help predict, measure, and control the process quality yields. The execution of the model should provide data for the analysis of assembly, test and repair strategies.

Each task must be met for a successful study. Figure 1 represents the life-cycle of the analysis. Fish-bone analysis is used to identify the cause and effect of faults in sub-assembly manufacturing and to collect the fault data to be used in the simulation model. The IDEF methodology is followed to develop a static model of the system. This static representation of the process provides the process data needed for the simulation. The process development teams are trained in IDEF to develop and to maintain the model, making changes as they occur in the process. Simulation modeling is used to understand the changes being made to the process and to evaluate the alternatives being considered. The simulation model is also used to determine the volume requirements for the process. These models are described in detail in the next three sections.

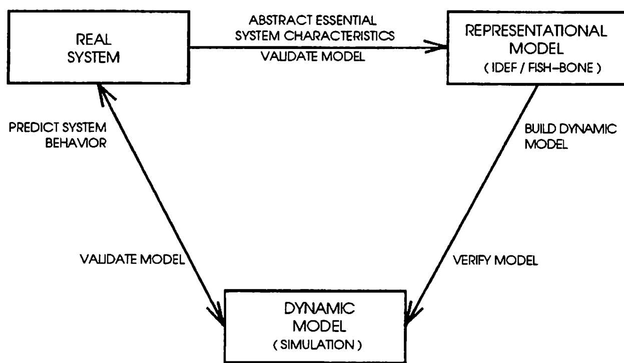

Figure 1. Life-Cycle of Analysis

2.1 Fish-Bone Analysis

A major inhibitor in the pursuit of higher yield levels lies in the difficulty of systematically and consistently identifying the many causes of faults in manufacturing. This difficulty in the sub-assembly manufacturing environment stems from many sources: the constant competitive pressure to bring our products to market, the inevitable changes in engineering design, the low volumes, and the common grouping and segmentation of the various assembly and test operations. A structured analysis method is needed to identify the types and causes of faults in the manufacturing environment. Fish-bone charts are used because they are easy to construct and provide a clear view of the relationships between faults and dependent variables.

The fish-bone charts identify 20 distinct defect types in sub-assembly manufacturing. Figure 2 illustrates the cause and effect analysis for poor bonding. The defect types (e.g. shorts, opens, solder balls) are the effects of poor bonding and are represented as branches off the main horizontal. Each of these defects are caused by other conditions which are drawn as secondary branches. The causes for shorts are shown in Figure 2.

Fish-bone charts identify the defect information to be included in the fault model. Brain-storming sessions are held with the design and process engineers to establish the complete fault model. The fault model consists of the following:

- incoming defects to the process in parts per million,
- defects induced by the process in parts per million,
- source of manufacturing fault where the defect was induced,
- defect capture points,
- and defect capture rates.

An example of the fault model for defect types shorts and dead dies is shown in Table 1.

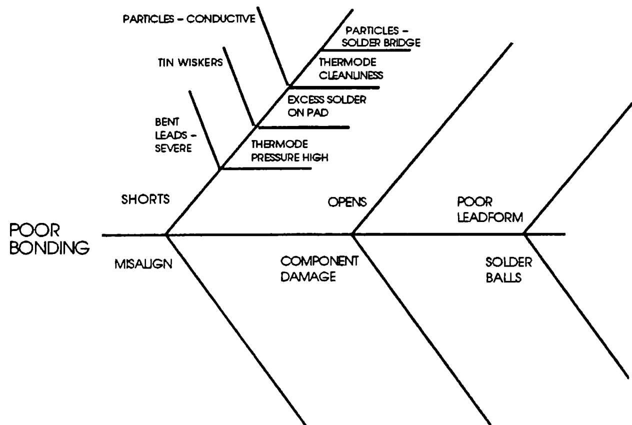

Figure 2. Fish-Bone Chart for Fault POOR BONDING

2.2 IDEF Model

The goal of the IDEF analysis is to develop a representational model which accurately describes the sub-assembly manufacturing process. Given that we are analyzing a new process at the prototype stage of development, we need a method that can easily communicate the changes that occur in the manufacturing process. IDEF helps us to understand the process and also helps in the development of the simulation model by providing a good conceptual model of the manufacturing process. The IDEF model is decomposed to the level required to build the simulation model. An example of the top level IDEF model of the process is shown in Figure 3.

2.3 Discrete Event Simulation Model

The discrete event simulation model is developed using SLAM II. One of the main criteria for the simulation model development is that the model should be flexible enough to allow for rapid changes in the manufacturing environment and yet be detailed enough to capture the whole process. The model logic should capture the defect propagation through the process at a sub-assembly, chip and lead level.

The model consists of a main section, which represents the process flow in the sub-assembly manufacturing process, and four modules representing defect generation, test, repair and analysis. The main section consists of the product routing, processing times for assembly operations, buffer sizes, and equipment requirements. Each entity (i.e. sub-assembly or part) that enters one of the modules is processed through the module according to the information carried with the entity. The modular approach helps keep pace with the changes which occur on a regular basis. Also, we can help the design team to understand how changes made to specific process step affect the whole process.

A wide variety of process data along with quality information is needed to run the simulation model. All requisite data needed for the simulation model is consolidated at one location in the model by storing all data in arrays and by using entity attributes to manipulate data from the arrays. This consolidation simplifies data entry .

The following sections provide a brief description of the four modules used in the simulation model. The four modules are the Defect Generation module, the Test module, the Analysis module, and the Repair module.

2.3.1 Defect Generation Module

We need to understand how quality or the lack of quality affects the process. A mechanism is defined to populate the

Table 1. Fault model for Defect Type Shorts and Dead Dies

Type of Defect	Source of Fault	Defect Rate PPM	Test Capture Point	Test Capture Rate	Defect Analyze Point	Time to Analyze	Defect Repair Point	Time to Repair
Shorts	Bonding	1000	Test-3	99.9%	Analyzer	20 mins	Touchup	4 secs
Dead Die	Incoming	100	Test-2	99.9%	Analyzer	40 mins	Replace	2 mins

entities entering the system with the various defect types. The entities are populated with all the defect types in parts per million (ppm) at the beginning of the process. This is the first module an entity encounters when it enters the system.

From the fault list we know the incoming defect rate, R, for every defect type. Depending on R, there is a finite probability, Y, that a part will have no defects of a particular type and this can be calculated using the binomial formula, Y=(1-R)**N. N represents the population and is used to model the defects at a sub-assembly, chip, and lead level. For example, each part coming into the manufacturing environment represents a chip, and each chip has, on average, 400 leads. A number of chips combine to form a sub-assembly. If we consider the defect type shorts, the population N for every chip is 400. If we consider the defect type dead chips, then the population N will be 1 at the chip level, and at the sub-assembly level N would depend upon the number of chips on the sub-assembly. Thus by manipulating N, we can model the three levels of defect population.

Using the finite probability Y, the defect generator module is used to separate the incoming entities into those containing a defect type, and those that do not. The entities containing the defects are then populated with a probabilistic number of defects. Some entities might have multiple defects of same type, some might have one, some two and so on. The defect rate for each defect type present is represented by the ppm level.

The other three modules, test, analysis, and repair, sort these defects according to the process characteristics and attach the resulting information to the parts for further processing. There are 20 defect types included in the model. Additionally, each defect can be captured in any of four sections depending on which process step is being performed on the entity. These sections are testable defects (TD), analyzable defects (AD), repairable defects (RD), and escaped defects (ED). Therefore, the model uses a 20 x 4 matrix to track the current defect information for each part flowing through the process. This results in a total of 80 pieces of information that are changed as the part flows through the process.

2.3.2 Test module

The first time that a part enters a particular test, any defects that are present have escaped all previous tests. Thus the ED section is the only section which has any information. All defects which might be captured at the test (i.e. the test capture rate for that defect type is greater than 0) are transferred to the TD section. All defects which cannot be captured at the test (i.e. capture rate equals 0) remain in the ED section. Each

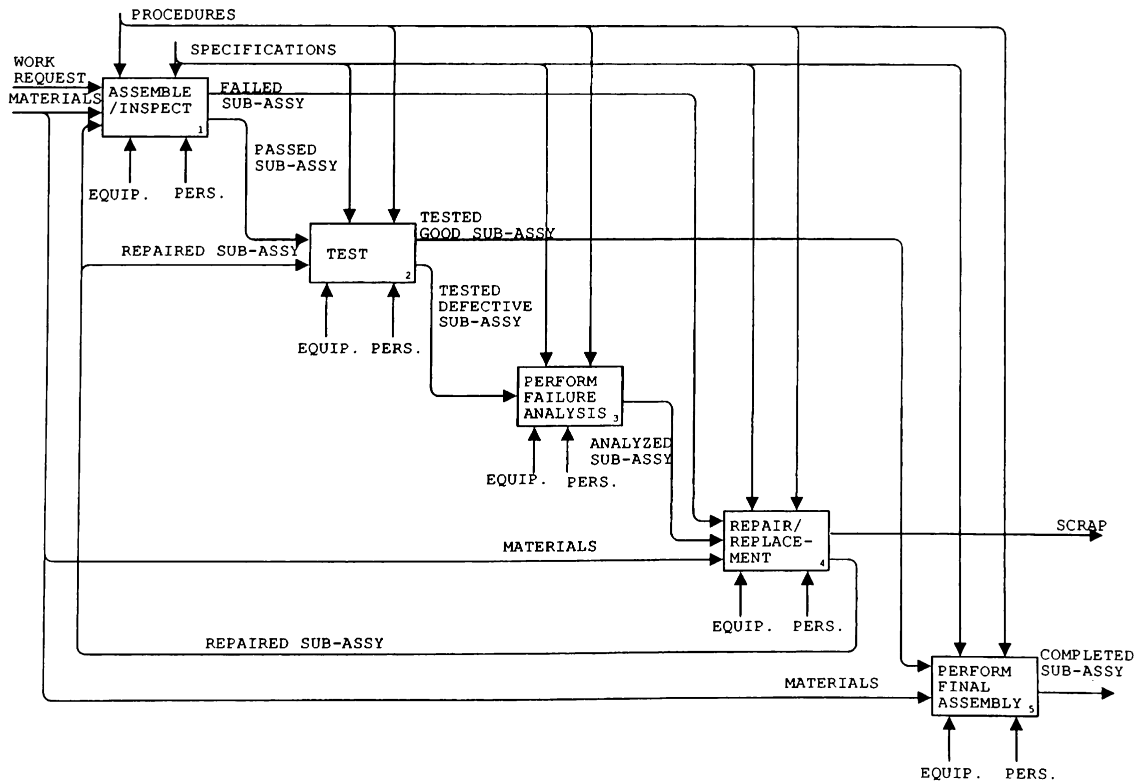

Figure 3. Top-Level IDEF Model of Manufacturing Environment

defect in the TD section is then tested and probabilistically gets captured or escapes. For example, if a test has a 50% capture rate for a defect type, a particular defect has a 50% chance of being captured and a 50% chance of escaping. If captured, the defect is added to the AD section for that defect type. If a defect escapes, the defect is put back in the ED section for that defect type. Once all the defects which can be tested have been tested, the part returns from the test module with a flag indicating whether or not there are any defects captured and a flag indicating that this test level has been reached.

2.3.3 Analysis module

The purpose of the analysis module is to verify and isolate the defect that has been identified by the tester. This module determines the time to analyze the captured defects that will be repaired and where this repair will take place. This is accomplished in the following manner. Upon entering the analysis module, the part has information stored in the AD section indicating the number of each type of defect that has been captured. Information is also available concerning the analysis time per defect by defect type, the maximum number of defects that can be analyzed before going to repair (threshold), and the repair station that will repair that defect type.

When the part enters the analysis module, the module searches through the AD section until it finds a defect. At that time, two things are recorded: the repair station where that defect type is repaired and the threshold value for that defect type. The module continues by analyzing the defects present. As defects are analyzed, the time to analyze each is calculated and added to the total time for analysis. The defect is then moved from the AD section to the RD section. This continues, bypassing defect types that are repaired at different stations, until either the threshold value is reached or until all the defects have been analyzed at which time the analysis is terminated.

Once the analysis is terminated, all the defects that have not been analyzed are moved to the TD section and the part returns from the analysis module with an indicator for the total time for analysis and an indicator for the repair station to which the part will be sent.

2.3.4 Repair module

The purpose of the repair module is to determine the number of analyzed defects that get repaired and the time required for the repair. When the part enters the repair module the defects that have been identified for repair are indicated in the RD section. Additionally, information about the time to repair per defect and the probability of repairing the defect is available in the repair station description for each defect type. Each defect is repaired individually. The time for each repair is calculated and added to the total repair time. Additionally, the defect is probabilistically either removed from the part or is moved back into the TD section. For example, if the probability of repair is 80%, there is an 80% chance that the defect will be removed and a 20% chance that it will not be repaired and will therefore be moved back into the TD section. When all defects in the RD section have been repaired, the part returns from the repair module with an indicator for the total time for repair.

3. RESULTS

The following section presents the simulation model inputs and briefly discusses some results from the simulation analysis.

3.1 Model Input

The model input consists of the process and fault information.

- Processing Information: The process information includes the standard process data of equipment requirements, processing times, product routing, station downtime, shift schedules, and buffer sizes.
- Fault Information: The fault information includes the results of the fish-bone analysis: defect types, defect levels in ppm, fault source, defect capture point, defect capture rate, test time based on defect levels, analyze point, analyze time based on defect levels, repair point, repair time based on defect levels, probability of repair, and threshold value.

3.2 Analysis Output

The output from the simulation model generates the standard simulation report identifying work in process (WIP), equipment requirement/utilization, cycle time, throughput. The output also contains fault information on defect escapes and process yield. Defect escapes are classified by defect types. The following graphs highlight some analysis findings.

Figure 4 shows the impact of defect levels on the number of pieces of equipment required to manufacture a certain volume of sub-assemblies. The graph represents the equipment required to manufacture a certain volume with base level defects in ppm versus a 25% increase in ppm levels for all defect types. Base defect level represents the average expected defect levels for all defect types in ppm. Given the high cost of capital in sub-assembly manufacturing, this type of analysis shows the cost of operating at different defect levels. This helps to prioritize capital investments to meet volume goals.

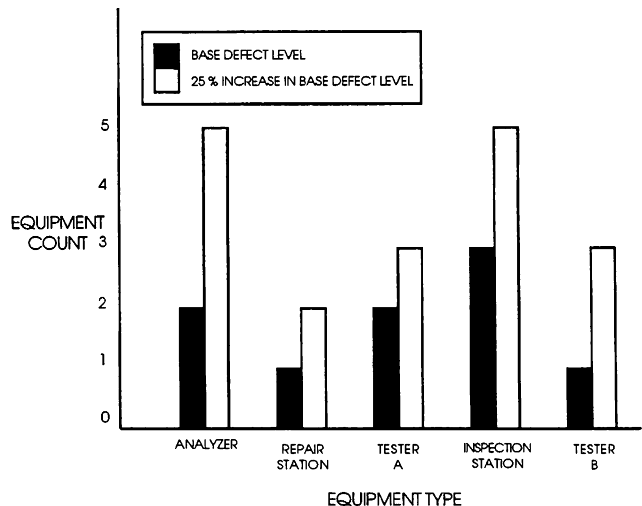

Figure 4. Impact of Defect Levels on Equipment Requirements

Figure 5 shows the impact on cycle time due to incoming material quality levels. The graph represents cycle time for different ranges of defect levels in ppm for defect type dead dies. This type of analysis helps in evaluating the impact of vendor quality levels, and is also used to study the impact of defects induced by the process. The equipment set is held constant in these scenarios. The analysis includes similar experiments which show the impact on other system variables (e.g. throughput, WIP, time in queue) by selectively increasing the range for certain defect types.

Figure 6 and Figure 7 show the impact of varying capture rates of the tester on defect escapes, cycle time, and throughput. The analysis includes an evaluation of similar scenarios by varying the capture rates on different test and inspection equipment. This type of analysis is used to evaluate various test strategies on the process.

The four graphs give a flavor for the type of analysis which is done using the simulation model. The analysis includes other scenarios to study the impact of defect levels on process issues such as WIP, buffer sizes, equipment utilizations, etc.

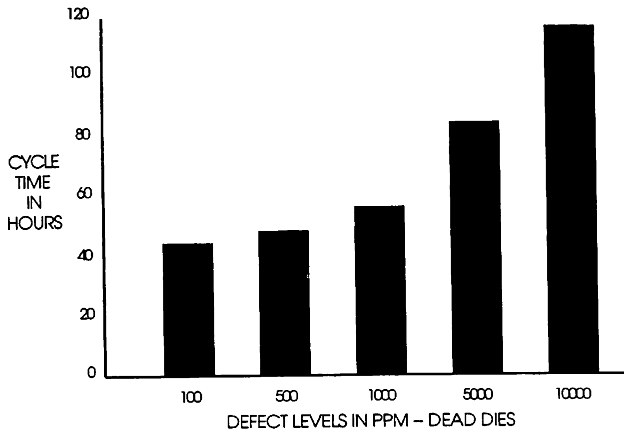

Figure 5. Impact of Varying Defect Levels on Cycle Time

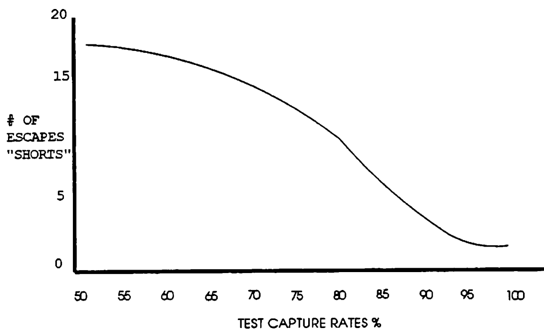

Figure 6. Impact of Test Capture Rate on Defect Escapes – SHORTS

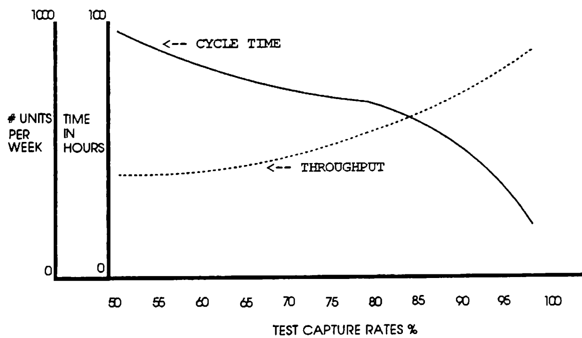

Figure 7. Impact of Test Capture Rate on Cycle Time and Throughput

4. FUTURE WORK

The results of this analysis work is being presented to different manufacturing groups within Digital. The analysis and results are valued and have generated a lot of positive feedback and interest. The manufacturing groups have expressed the need to continue to use this type of analysis in process development. Interest has been expressed from different groups to develop the simulation model as a dynamic modeling tool with a user-friendly interface to allow for the model to be used by manufacturing engineers with a basic understanding of simulation. The possibility of a dynamic modeling tool to study a process from both a quality and a capacity point of view to evaluate different process strategies has fostered support from the different organizations within manufacturing. We are currently working on a project to develop the tool.

5. CONCLUSION

In this paper we describe the analysis work done to augment concurrent product and process engineering. We use a suite of tools to facilitate the communication between the various groups in the process development effort, including simulation to analyze a process both from a capacity and quality standpoint. The analysis is used to formulate the volume process strategy for the new sub-assembly manufacturing process. Our future work would ensure an easy-to-use tool that would help in prioritizing and identifying opportunities in manufacturing and in new process developments.

GLOSSARY OF SELECTED TERMS

Capture Rate: The probability of capturing defects.
Threshold Value: The maximum number of defects analyzed and repaired in one pass through the process. The threshold value is attained when the level of defects is reached, which makes additional analysis ineffective until those defects are repaired.
Probability of repair: The probability of repairing a defect without inducing one.
Electronic Sub-assembly: A populated substrate. e.g., Modules.
Breadboards: A hardware model of the actual system.
IDEF: A structured methodology to represent activities in a process.
Dies: Silicon wafers.

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