CLASS SIMULATION OF REAL TIME, HIGHLY COMPRESSED VIDEO TRANSMISSION THROUGH AN INTERFERENCE LIMITED ENVIRONMENT*

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ABSTRACT

CLASS (Communication Link Analysis and Simulation System) has been modified to predict the performance of digital video telemetry systems in remotely controlled spacecraft robotics applications where the communications link may be highly corrupted by RFI (radio frequency interference). Unlike previous functional type simulations which use statistical models to characterize the steady-state channel, this new CLASS tool is an emulation type simulator which is capable of modeling both transient and steady-state conditions in the channel. The system architecture uses sequential tasking to simulate bit-by-bit signal processing through each successive component of the channel. Subsystems are: 1) the digital video data compression and reconstruction subsystem; 2) the Reed-Solomon Codec subsystem; and 3) the TDRSS Link subsystem. Subsystems 2 & 3 form a concatenated coded channel using a Reed-Solomon outer code and a convolutional inner code. The novel features of the software package are: 1) the modular design offers easy modification of the system configuration; 2) it provides extensive performance characterizations of channel components and subsystems including loss of synchronization and reacquisition; 3) through statistical reduction and transformation of emulation type simulation data bases, the simulator may be reconfigured to a speedy, efficient functional type simulation. This paper describes the capabilities, structure and modeling techniques of this new version of the CLASS as it is used in modeling the Orbital Maneuvering Vehicle (OMV) video telemetry return (VDTLMRTN) channel.

1. INTRODUCTION

As NASA advances into the space station era, the applications for video sensory remote control system using RF telemetry links in the control loop are entering the detailed parametric design phase. NASA/GSFC's Communication Link Analysis and Simulation System (CLASS) [1] provides a sophisticated high fidelity computer aided design and analysis tool by which the required video telemetry links performance parameters may be determined.

The Orbital Maneuvering Vehicle (OMV), a logistics support component of the space transportation system (STS), is currently under development. The OMV is a robot type spacecraft that is remotely piloted from the ground. It is designed to service other spacecraft and will use multi-camera viewing of the target spacecraft to support the pilot's control during surveillance and/or docking maneuvers [2]. The Tracking & Data Relay Satellite System (TDRSS), the space segment of NASA's Spaceflight Tracking & Data Network (STDN) [3], will host both the OMV's video telemetry return (VDTLMRTN) channel and the OMV's command forward channel via the S-band single access (SSA) link subsystem. SSA links are subject to corruption by a variety of random noise and by radio frequency interference (RFI) resulting from ground based S-band emitters appearing in the field of view of the TDRS's S-band single access antenna during OMV service.

Due to high-ratio digital-data-compression operations in the OMV Video Compression Units (VCU), errors introduced during the transmission through the VDTLMRTN channel, if uncorrected, will tend to propagate thus seriously corrupting the video image reconstructed by the Video Reconstruction Unit (VRU) in the ground station. This error sensitivity problem leads to the specification and implementation of a concatenated coding system using an interleaved

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Reed-Solomon (RS) code as the outer code and the standard TDRSS convolutional code as the inner code.

The use of the video link is so critical to the OMV's remotely piloted operation that it made necessary the development of a simulation tool capable of providing a reliable simulation data base by which to assess the capability of video compression/reconstruction techniques to withstand the TDRSS RFI environment when using the error correction and containment capabilities designed into the OMV VDTLMRTN channel.

This paper describes the CLASS-OMV, a software package simulating the VDTLMRTN link performance, in terms of its modeling approach, its capabilities and its software structure. Section 2 discusses the modeling approach for a bit-by-bit emulation type of software for the VDTLMRTN channel. Section 3 describes the CLASS-OMV statistical processing to obtain the performance statistics. The CLASS-OMV software structure is explained in Section 4. Finally, Section 5 discusses further potential application of the bit-by-bit emulation system modeling.

2. CLASS-OMV VDTLMRTN CHANNEL MODELING

The CLASS-OMV VDTLMRTN Channel Simulation System (Figure 1) is a time domain model. The digital signal processing components of the system are directly emulated in their processing functions. The VCU & VRU Subsystem and the R-S Codec Subsystem assign each bit a single binary representation. In the TDRSS Link Subsystem, the convolutional encoder, periodic convolutional interleaver and cover sequencer (PCI) represent each code chip with a single binary digit. The de-periodic convolutional interleaver and de-cover sequencer (de-PCI) accepts data from the 8-ary quantizer of the detector output and represents each receiver code chip estimate as a 3-bit PCM code. The Viterbi-algorithm decoder (VA decoder) output is one binary digit per data bit.

In the RF Link Subsystem, each convolutional code chip is represented by eight phasor samples. Monte Carlo simulation is employed to simulate corruption of the phasors in the channel.

The structure of the software is sequential task module oriented. The major task modules in CLASS-OMV VDTLMRTN are depicted as blocks in Figure 1. Each block is an individual task module and is operated by a

control module called RUN CONTROL. When a task module is activated by the RUN CONTROL it reads data from its input data file (indicated with .DAT suffixes) and executes the bit-by-bit hardware emulation on the signal data while logging both signal and hardware performance data for later calculation of the statistics at several crucial points in the task module.

Upon finishing processing, the processed signal data is written into its output data file. The data file, specified by *.DAT, serves as the output data file to the previous block and as the input data file to the following block. As shown in Figure 1, a data file exists between each pair of task modules.

The first data file, INVIDEO.OUT, contains the actual digital image data which will be emulated through CLASS-OMV VDTLMRTN channel to obtain the reconstructed digital image data stored in the last data file, OUTVIDEO.DAT. The data collected in each file contains both the data bit and the task module performance information to allow both the reconstruction of image data and the prediction of various performance characterizations by CLASS-OMV Statistical Processing Control which will be discussed in Section 3.

Simulations using CLASS-OMV VDTLMRTN, are done in two major computing cycles: a channel simulations cycle and a data processing cycle (Figure 2). Both cycles are configured parametrically in one set-up operation. All simulation parameters are input into the RUNDB.DAT file, the run control file which governs the entire simulation.

A special short cycle feature -the picture previewallows the operator to screen the video data base in INDVIDED.DAT and to customize the order of scenes being input to the channel. This feature provides the ability to simulate each camera viewing different space scene data in multi-camera modes for the video telemetry system. This gives enormous benefit to systems engineering studies to establish piloting control algorithms in advance of actual maneuvers. The high fidelity software modeling of the bit-by-bit hardware emulation for the major subsystems is described as follows.

2.1 VCU-VRU Subsystem

The software for the VCU-VRU subsystem employs the fundamental algorithms developed by Fairchild-Western Systems Incorporated for NASA [4] and

CLASS-OMV VDTLMRTN SIMULATION SYSTEM FIGURE 1:

is used as the primary hardware design tool for the OMV video data compression system. In CLASS, the software was modified to operate in sequential instruction machine, interface with the R-S encoder/decoder, made flexible for configuration selection and fitted with system diagnostics routines.

The CLASS software models only that portion of the video data compression system which is encompassed in the VCU. CLASS-OMV is capable of emulating the OMV VCU & VRU hardware operation in several of its various camera modes, resolution modes, and subframe formats.

The VCU performs the compression of digital video data in three ways: Pixel pairing, differential PCM encoding, and entropy encoding. In the dual camera mode, 8-bit-per-pixel digital image data is created at the OMV cameras at the rate of 19,910,400 bps. This video data is then processed by the VCU to achieve a data rate to the RS encoder of 907,200 bps. A twenty-two-to-one compression rate is obtained by VCU data compression algorithm. A picture frame is further divided into several subframes. Each compressed subframe contains sufficient overhead information to identify its position in a picture frame and to enable VCU synchronization for subframe reconstruction together with the space image segment.

The VRU emulates the video reconstruction process which includes entropy decoding, DPCM decoding and spatial interpolation. A subframe will be replaced by the one in the previous frame in the case an error is detected within the subframe. Both the entropy decoding and an undecodable data flag generated from RS decoder provide information for subframe replacement.

2.2 Reed-Solomon Codec Subsystem

The Reed-Solomon Codec Subsystem is a generic tool to simulate a Reed-Solomon type block encoder/decoder. It can be internally configured to use various generator polynomials in constructing the code. For the OMV system, it is configured to the encoder/decoder architecture developed by Cyclotomics incorporated for the OMV [5].

This subsystem contains a (255,238) Reed-Solomon (RS) code together with a helical interleaver with a depth of eight R-S codewords. Within each RS codeword, there are 16 parity-check symbols combined with 238 information symbols thus enabling the decoder to correct up to 8 erroneous symbols in a codeword. The

255 symbol code block is obtained by appending a sync symbol at the end of each RS codeword to provide the RS block synchronization.

As a true emulation type of simulation, the bit-serial RS encoder first groups 1904 bits from its input data file and then encodes these 238 information symbols to generate an additional 16 parity symbols. The encoded codeword is stored in its output file, which is used later by the helical interleaver as its input data file. The RS decoder performs the Berlekamp iteration algorithm to decode the received and deinterleaved codewords provided with codeword boundary information as acquired by the RS block synchronizer. In the case where an undecodable error pattern is present, the RS decoder will also store in its output data file an undecodable data flag which provides information for the VRU to process the video reconstruction.

The helical interleaving is used to randomize burst errors created by the Viterbi decoder [6]. With the eight RS codewords interleaving-depth the RS decoder will be able to correct an error burst of length 505 bits. Several advantages of using helical interleaving are listed as follows:

- i) Helical interleaving can provide RS decoder the capability of burst forecasting which may double the burst error correction capability.
- ii) Compared to block interleaving, helical interleaving requires less memory, less interleaving delay and less acquisition time.
- iii) It causes no additional burden for the RS block synchronizer.

The RS block sync acquisition algorithm employs an 8-bit window sliding along the received data at the output of the Viterbi decoder. Successful sync acquisition is declared only after the detection of the sync symbol several times at proper intervals. The number of sync detections required depends on the threshold setup of the synchronizer. A high threshold setup usually results in a long acquisition time, but reduces the probability of false lock. After sync declaration, the correct codeword boundary information is stored in its output file, and used by both the helical deinterleaver and the RS decoder for successful operation.

2.3 TDRSS Link Subsystem

The TDRSS Link Subsystem is further divided into the Convolutional Codec Subsystem and the RF Link Subsystem. The Convolutional Codec Subsystem is a generic tool to simulate convolutional encoders and

maximum likelihood decoders; however, it can be configured to emulate the TDRSS high-data-rate decoder as developed by M/A-Com Linkabit [7]. The Subsystem contains a convolutional encoder, periodic interleaver/deinterleaver, PN cover sequence/de-cover sequencer, synchronization detector, and Viterbi Algorithm decoder. The convolutional code employed is a rate 1/2, constraint length 7, nonsystematic, transparent code which can provide a coding gain of 5 dB at bit error rate of 10⁻⁵. The interleaver/deinterleaver is a (30,116) periodic interleaver which is available for use when the channel errors are bursty. The interleaver/deinterleaver allows any two convolutional code symbol chip errors within a group of up to 120 symbols to be separated by 30 symbols.

The decoder/deinterleaver synchronization is achieved through the use of a cover sequence, applying at both the interleaver and deinterleaver, and a decoder sync detector. The sync detector monitors the minimum metric rate of growth within the decoder to determine the in-sync or out-of-sync condition. The decoder/deinterleaver performs a spiral search algorithm once the decoder out-of-sync is declared.

The RF Link Subsystem contains the transmitter, RFI source, relay satellite (TDRS) and receiver modules. The transmitter task-module contains a BPSK/QPSK modulator, power amplifier and transmit filter. The relay satellite task module contains a limiter, filter and power amplifier. The receiver task-module contains pre-detection filters, carrier recovery loop, bit-timing recovery loop, matched filter and a 8-level quantizer. A detailed description of the above modules is in [8]. The RFI source models the RFI as a Poisson process. The arrival rate and power level are determined based on true measured RFI statistics.

The approach of emulating and collecting user data bit-by-bit in CLASS-OMV usually requires much larger data bases than required for the functional approach. Nonetheless, significant advantages derived from this true emulation approach are as follows:

- 1) It serves as not only an analysis tool but also as a design tool through the flexibility it offers to easily alter individual blocks in the simulation system and observe the effects on the overall system performance. Each block module can be modified and tested separately to accommodate system hardware changes. Block modules can also be removed and new module may be inserted to simulate system build-up and test.
- 2) As a complete mission model, it can be used to evaluate both the static and dynamic channel environ-

ments. It is, particularly, capable of simulating the synchronization transients in a concatenated coding channel for the receiver, the V.A. decoder and the RS decoder

3) It provides the capability of high speed functional simulation. The user data collected in an end-to-end full emulation simulation can be post-processed, described in Section 3, to obtain both bit error and synchronization statistics. Based on these statistics, statistical error generators are developed and applied in several layers of the simulation system to functionally simulate the corresponding channel. Figure 1 shows statistical error pattern generators for the TDRSS Link (including VA decoder) and for the end-to-end concatenated coding channel. The tendant problem of extensive computation in the emulation simulation is thus solved by functional simulation under the same channel conditions in a speedy, efficient method.

The CLASS-OMV VDTLMRTN channel simulation system is configurable through the run control to utilize either the full emulations simulation approach or the functional simulation approach. Three featured configurations are as follows:

Configuration 1. Full emulation simulation, end-to-end.

Configuration 2. Functional simulation of the TDRSS link with emulation of the RS subsystem and VCU-VRU subsystem.

Configuration 3. Functional simulation of the concatenated coding channel with emulation of the VCU-VRU subsystem.

3. STATISTICAL PROCESSING

As stated previously, a CLASS VDTLMRTN simulation is performed in preliminary cycle followed by two main cycles where each cycle employs multiple task modules in its execution. The second main cycle is the data processing cycle which is normally referred to as the statistics processing cycle, although, it has several non-statistical functions [8].

Based on the channel simulation data collected in *.DAT data files, CHANNEL PERFORMANCE PROCESSING evaluates the bit error rate (BER) and synchronization performance by manipulating the related data files. Some of the performance statistics are used to characterize and verify the software modeling while other statistics provide information both to validate the OMV video and communications system

design and to define allowable RPV operational parameters. Output data listings and plotting capability is provided for various tables, histograms, and other statistics versus EIRP margin (a derivative of channel signal-to-noise) for the RFI environment selected.

3.1 BER Performance

Bit-Error-Rate, BER, is typically the primary measure of a random channel's digital transmission performance. For the CLASS VDTLMRTN simulations, BER is calculated at three different levels of a concatenated coding system: the uncoded error rate; the convolutional-encoded-Viterbi-decoded error rate; and the concatenated coded output bit error rate. Not only random errors but also burst errors are modeled in each level using the concept of guardspace. Any two erroneous bits symbols with less than the selected guardspace of error-free bits between them are considered to be in the same burst. Typical burst statistics are depicted in Figures 3,4,5 and 6. Based on the statistics of burst length and erroneous bits within a burst, a statistical burst error generator can be developed with high fidelity for the TDRSS Link (including VA decoder) and the concatenated coding channel given sufficient burst statistics. These burst error generators allow high speed bit-by-bit functional simulation.

3.2 Synchronization Performance

Channel synchroniation for the OMV's VDTLMRTN concatenated coding channel involves carrier synchronization, bit synchronization, de-PCI cover sequence synchronization in conjunction with VA decoder, helical deinterleaver synchronization in conjunction with R-S decoder, and finally VRU synchronization. The CLASS allows simulation of sync loss/recovery transients for any of their five levels of channel synchronization.

For bit sync statistics, the clock timing error and clock jitter spectrum are evaluated. Two sources to cause sync loss at the Viterbi decoder - PCI sync detector, are a bit slip which gives true-sync dropout and false alarm which is more severe since it would, in general, take a much longer time to regain sync due to the cover sequence spiral search algorithm modeled in the software. Both the initial acquisition time and reacquisition time required for sync losses are evaluated together with probability of bit slip and false alarm. The same type of synchronization performance is evaluated for RS block synchronizer. The synchronization statistics evaluated for RS block synchronizer provide a basis for evaluating the threshold selection of

RS block sync and thus controlling the acquisition time.

3.3 Video Reconstruction Performance

The CLASS is capable of accepting true or simulated video data and processing through the VDTLMRTN channel and then displaying both the original image and the processed/reconstructed image on a video monitor for viewing of the channel performance. Figures 8 and 9 illustrate this capability. Subjective visual examination by the OMV pilot can be applied to evaluate the acceptability of the reconstructed picture shown in the monitor. Objective performance evaluations of the reconstructed image quality are also provided such as: subframe replacement counts and pixel error counts.

4. CLASS-OMV SOFTWARE STRUCTURE

The CLASS VDTLMRTN channel simulation system software architecture is comprised of four task drivers implemented in separate Fortran programs as shown in Fig.2.

The first task driver is an interactive operator interface by which a simulation is set-up and controlled. After setup this outer controller selects the next level task driver from: picture preview, VDTLMRTN channel simulation run or performance statistic run. More information regarding each type of the run is then requested from the operator to create a run data base.

The second level task driver, PICTURE PREVIEW, displays the selected picture on the screen allowing the operator to preview and decide the pictures to be processed by VDTLMRTN simulation system.

The second level task driver, VDTLMRTN CHAN-NEL SIMULATION, performs a VDTLMRTN simulation based on the run data base created during run setup. The run data base contains system configuration information and typical VCU and TDRSS channel parameters. A bit-by-bit emulation or functional simulation is then performed for either an end-to-end or truncated link.

Finally, the second level task driver, CHANNEL PERFORMANCE PROCESSING processes the collected simulation data in each data file to obtain a wide variety of performance statistics. This task driver

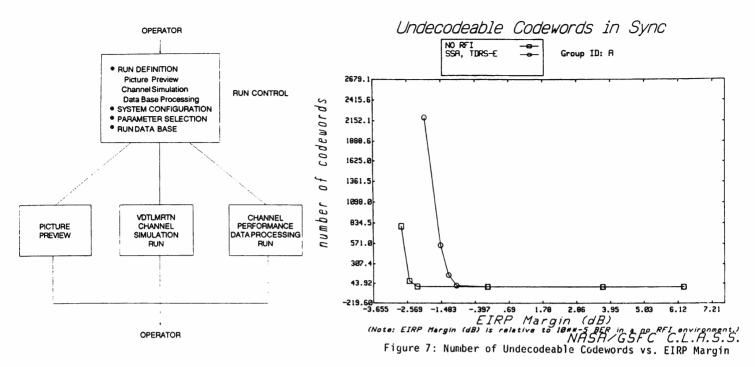
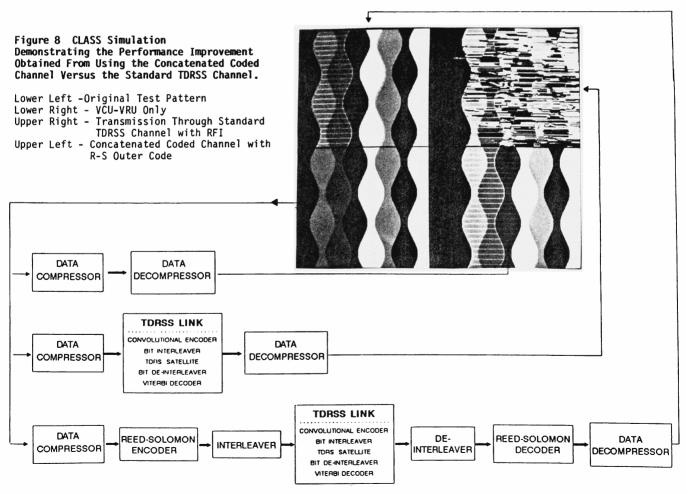
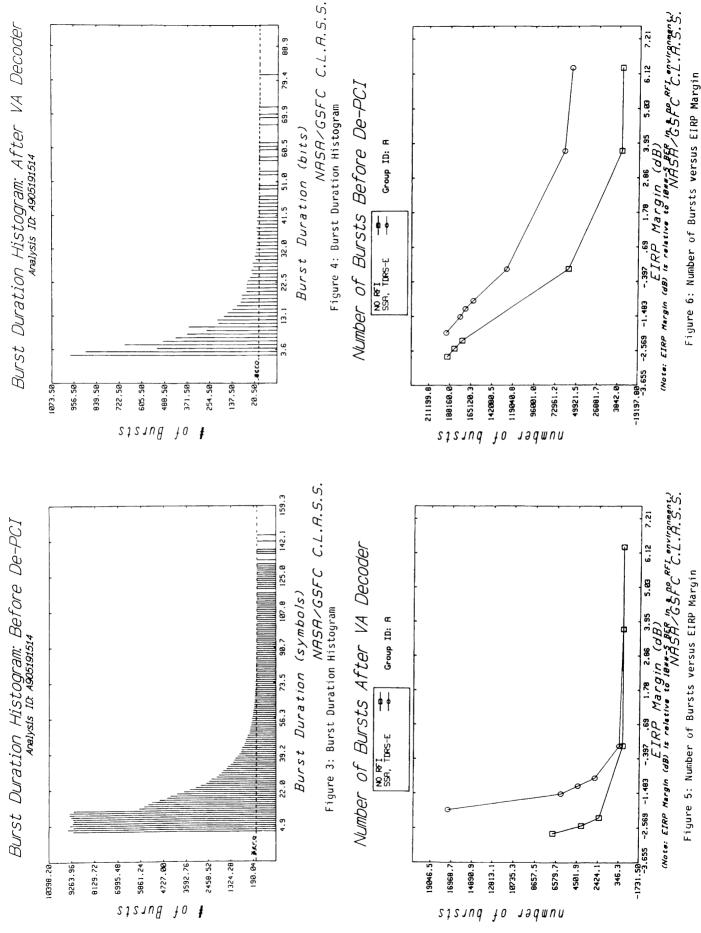


Figure 2: CLASS-OMV Software Structure





may utilize any 10 channel performance data processing task modules which perform in a manner analogous to the channel simulation task modules. A few selected examples are given in section 5.

The program employs adaptive heuristics. When called, each task module configures itself to the current simulation requirements. During software development true systolic processing was the initial choice. It was discovered, however, that maintaining continuity of the data convolution with the task module state required exhaustive prediction of the convolutional status for all possible systolic intervals. The problem was solved by taking the limiting case in which each task module, when called, pumps its complete input data file through its processing to the output data file.

5. SIMULATION OUTPUT DATA DEMONSTRATIONS

The ten task modules under control of the CHANNEL PERFORMANCE PROCESSING task driver provides extensive capabilities to make both point-to-point comparative characterizations and single point characterizations of the VDTLMRTN channel performance. One of its most advanced features is the ability to do trending characterizations thus producing a design oriented channel characterization. A few examples are discussed in the following paragraphs. The examples given are for illustration only and they represent only a sampling of the CLASS OMV capabilities.

5.1 Steady-State Burst Error Performance Analysis

Steady-state denotes a channel condition in which all levels of synchronization are "in-lock". Figures 3,4,5 and 6 illustrate characterization data for the burst error performance of the VA decoder in a steady-state channel.

Figure 3 shows a histogram type plot describing the numbers of error bursts versus the burst duration as measured at the 8-ary quantizer input to the de-PCI. This plot was reduced from the data logged by processing 200 frames of compressed video through the channel when corrupted by a high RFI environment while operating with a - 2.75 dB EIRP margin.

EIRP margin is the channel normalization scheme chosen in a format to allow the system designers to asses the space vehicle's transmit power requirement.

The EIRP margin is calculated relative to that value of EIRP which would produce a 10⁻⁵BER with rate 1/2 convolutional encoding.

Burst errors are distinguished from random errors by the guard space technique. The task mode which computes the burst error counts makes a point-to-point comparison of data held in the QUANSYNC.DAT file to data held in the PCI.DAT file.

The ability of the combination of the PCI/de-PCI and convolutional codec components to mitigate the RFI induced burst error corruption may be assessed by comparing figure 4 to figure 3. Figure 4 provides a histogram describing the burst performance at the VA decoder's output. It is readily observed that the number and duration of burst errors occurring at the VA decoder output is dramatically reduced as a result of the error correcting capabilities provided by the codec system. It should be noted that the burst errors at the VA decoder do not represent input bursts which pass through the decoder. Instead, the output bursts are entirely different as a result of the nature of the VA decoder. The system engineer may assess the character of these bursts (figure 4) and note that the maximum length burst at approximately 80 bits is well within the error correcting capability of the R-S decoder to follow in the channel: however, the closely spaced bursts may create a problem.

Figures 5 and 6 provide trending curves showing the results of twelve channel simulation runs of the 200 frame size described earlier. The channel variables for the trending curves are both the RFI environment and the EIRP margin. As expected, the no RFI channel performs much better at low EIRP Margins than the TDRS-E RFI corrupted channel. As EIRP margin is increased, the channel performance converges, becoming independent of RFI.

The performance of the R-S decoder may be assessed from the trending curves in figure 7. The data point on the high RFI curve at 2.75 dB EIRP margin corresponds to the burst error histograms data in figures 3 and 4. It is seen that although the maximum burst length (80 bits) shown in figure 4 was correctable by the R-S decoder, the composite of all the bursts combined with random errors (not illustrated) produce too corrupt a channel for the R-S decoder to mitigate. The R-S decoder finds over 2100 received code blocks with uncorrectable errors. From the trending data, it is seen that increasing EIRP margin eliminates the problem. Interactively comparing trending data in figures 5 and 6 to that in figure 7 allows defining the minimum channel

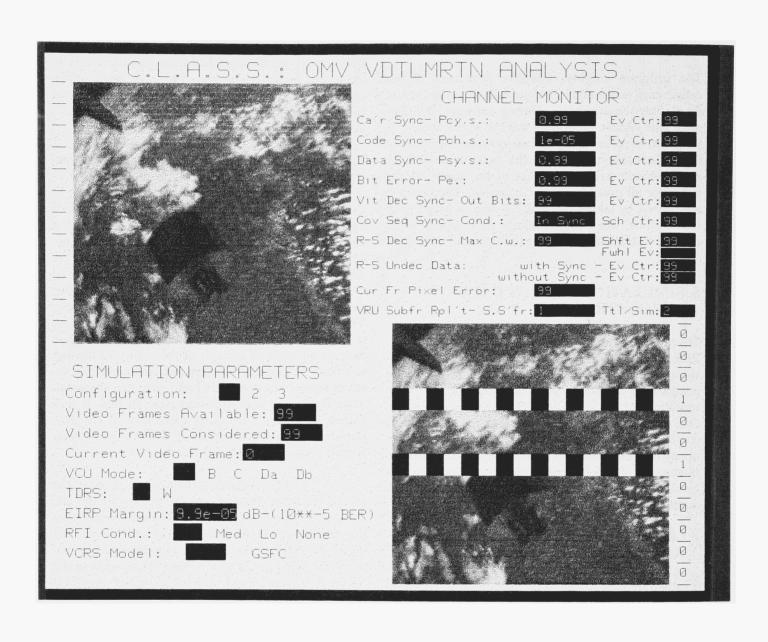


Figure 9 CLASS Video Monitor Display
Space Scene (upper left) versus
Reconstructed Image (lower left)
for the OMV VDTLMRTN Analysis

EIRP margin. Also note that in spite of the channel corruption, sync was maintained.

5.2 Video Reconstruction Analysis

Video displays not only dramatize the utilization of the simulation tool but also provide the best and final means of gauging the channels performance. Figure 8 illustrates a comparative simulation to demonstrate the effectiveness of the concatenated coding channel as compared to the standard TDRSS convolutional coded channel and to a simple loop-back operation of the VCU-VRU. Inspection reveals that when using only the convolutional coded channel, the reconstructed video is highly corrupted (when subframe replacement is not utilized). The addition of the R-S outer code restores clarity equivalent to that of the loop-back.

Figure 9 displays the actual CLASS monitor screen. The bars in the reconstructed image represent subframe replacement events due to corruption in the channel. The VCU is initialized with a bar pattern in the output video frame. The original input space scene is shown in the upper left corner. The INVIDED.DAT data file in this simulation exercise contained scenes from a space-shuttle satellite deployment operation.

6. CONCLUSION

This paper has described and demonstrated a powerful new addition to the CLASS of NASA/GSFC, the VDTLMRTN Channel Simulation System. This new computing tool offers greatly expanded capabilities to perform system level analysis and design tasks for coded communications links. It has been shown to be particularly useful in performing system trade/design studies for application of compressed digital video to remotely piloted space vehicles which will be required for future robotic operations in space explorations and development.

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