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SIMULATION AND ANALYSIS OF A CIRCUIT BOARD MANUFACTURING FACILITY

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ABSTRACT

A simulation model is used to analyze the effects of various factors on the performance of a complex manufacturing system. The system under study is a large circuit board manufacturing facility. There, circuit boards are assembled and tested on a wide variety of automated machines and manual workstations. The simulation model, written in the SLAM II language, is highly detailed in the manner in which processes are modelled. This becomes especially important in modelling circuit board testing where boards which fail are repaired and recirculated through the test stations. Detailed modelling also allows for numerous process routings among the different product types to be permitted. The model possesses a demonstrated accuracy in its portrayal of the real-world situation.

To make the most economical use of the model in the investigation of factor influence on system performance, experiments were conducted according to the principles of statistical experiment design. A 32-trial Hadamard design was employed to test the effects of such variables as lot size, order release schedules and quality on system performance. Performance measures included mean percent of work behind schedule, process flow time and in-process inventory levels. Significant results from these experiments are presented along with a set of guidelines, with respect to the factors investigated, which yielded favourable system performance results.

1. INTRODUCTION

Manufacturing simulation efforts reported in the literature are most often concerned with studying the effects of complex analytically-derived or heuristic production planning and control policies on relatively small-scale and well-controlled manufacturing systems. Examples include Holloway and Nelson (1974) who investigated a series of job shop scheduling heuristics in a simulated shop consisting of up to seven machines and up to fourteen jobs; due date setting and job sequencing algorithms were evaluated by Baker and Kanet (1984) for a four-machine shop; and a real time scheduling scheme which was studied by Gershwin, Akella and Choong (1985) by simulating a four-machine flexible PCB assembly system. The research to be described in this paper took a slightly different approach. Rather than starting with a new and complex mathematical production control strategy and developing a simulation model with which to study it, we started by creating a simulation model of a complex manufacturing system. We then conducted simulation experiments in which relatively simple production control policies were altered and their effects on the system gauged in an effort to gain a deeper understanding of the operation of the system and its components.

The simulation study was motivated by preliminary research conducted at a PCB assembly and test facility. Our research group at the University of Waterloo was invited to examine the manufacturing system and identify opportunities for improved production efficiency both in terms of material and information flows. During the course of the investigation questions arose which could not be answered. We identified two major problems: persistently high work in process levels and difficulties in meeting the production schedule. The use of simulation as a vehicle for probing these problems was suggested, and the modelling and analysis project reported here was initiated.

'Large scale' and 'high degree of complexity' accurately describe the manufacturing system under study. The facility which was modelled assembles and tests a wide variety of circuit board products which are used in computers and their peripherals. Approximately 80 assembly and test machines and workstations produce over 300 different product types in total quantities exceeding 1.5 million units per year. Many of the assembly and test operations are highly automated and computer-controlled, while others are essentially manual operations. For the purposes of the simulation exercise, 111 product types with combined volume of about 1 million units per annum are modelled. These products represented the relatively low-volume/high-variety product mix for the plant; the high-volume/low-variety component was not modelled. Each of the 111 different product types has a potentially different production process associated with it as well as a set of unique operation times for each stage in the process.

Assembly of PCBs in the plant is a relatively straightforward process. Bare circuit boards are populated with components of various types in a series of operations carried out on either automated machines or at manual workstations. PCB assembly is carried out in batches. Testing of circuit board assemblies is more complex. Assemblies must undergo a variety of tests. At each test there is a probability that a given board will fail and

require repair and retesting. Often, a board will cycle through a number of test-repair-retest iterations before it is defect-free. In the meantime, the boards which have passed the tests are sent ahead to the next operation. In the test phase of the manufacturing process, therefore, batches may be split.

To model the basic production situation, a network framework was chosen. Within this framework, entities (i.e., batches of boards) flow from one operation to the next with routing controlled according to each product's production process. As a basic framework, the network sufficed; however, it was foreseen that a large amount of activity external to the network structure would be necessary in order to model the subtleties of the production facility. Examples of this include the use of data which had to be accessed from data files outside the network. A simulation language was therefore required which combined network modelling with the ability to employ non-standard, user-written discrete events. The language which was chosen was SLAM II (Pritsker and Associates, West Lafayette, Indiana). In addition to the network/discrete event orientation of SLAM II, the detailed statistical output obtainable through this language was seen as an important asset.

In the remainder of this paper, the production process studied is outlined, and then some of the more interesting simulation techniques used in modelling it are presented. Next, the verification and validation stages of model development are discussed. The simulation model was used to determine the effects on production efficiency of production control policies such as order release frequency, lot size, job selection priority rules, amount of overtime worked, as well as quality levels. Measures of production efficiency included process flow time, work in process levels and the percent of jobs finishing production behind schedule. The policies and measures are discussed along with the statistical methods used and the experimental strategy employed to extract the most information from the model using the smallest possible amounts of time and computer resources. Finally, insights gained from the modelling and analysis project are shared.

2. THE PRODUCTION PROCESS

What follows is a brief description of the production process followed by a typical circuit board assembly through the manufacturing system (see Figure 1). It is organized along the lines of the production departments as modelled in the simulation.

Production Order Release: The timing of the release of production orders, as well as their size, is controlled by a materials requirements planning system. In the base case, release occurs on a weekly basis. This means that all production orders hit the floor on Monday mornings, due for completion on a Friday afternoon 5, 10, 15, 20 or 25 days hence, depending on the assembly's production leadtime. The model allowed for daily release as an alternative: orders were still due on Friday afternoons, but a more realistic leadtime (not rounded to the nearest five days) was used such that release could be scheduled to occur on any day of the week. Large orders are released as a series of smaller production lots. Maximum allowable lot size is a parameter of the model, but is controlled in actuality so that no lot is larger than that which can be processed at a production workcentre within the span of a single shift.

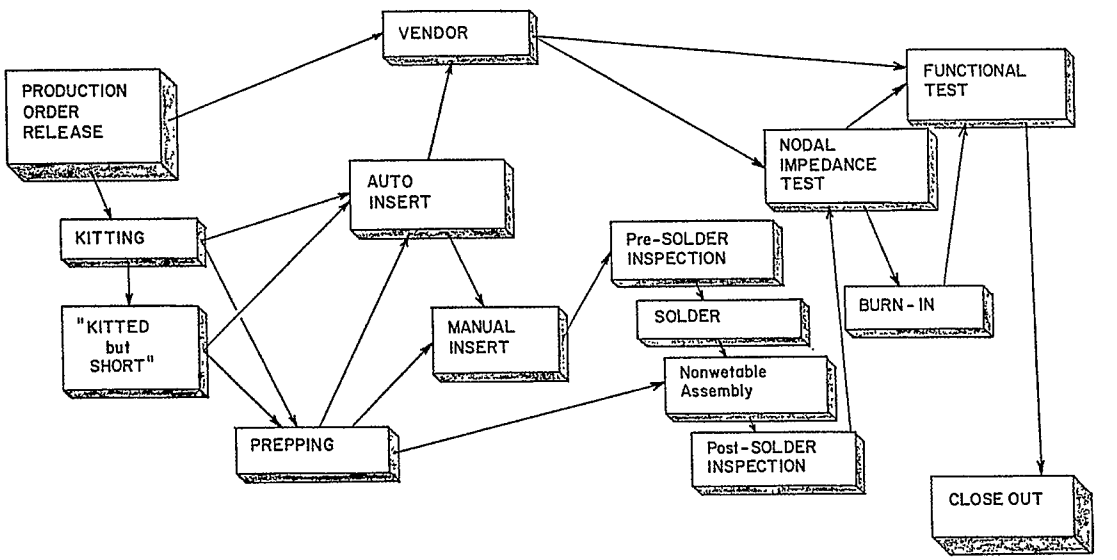

Figure 1: Production Process Routings

Kitting Department: Components required for PCB assembly are marshalled into kits. When component shortages are discovered during the kitting process, the kit is set aside to wait for the delinquent components. Some kits leave the kitting department with hidden shortages which are discovered only once the lot has entered the production process. The discovery of shortages in production causes delays. From Kitting, certain components are sent directly to the Automated Insertion department, while others are routed to the Prepping department.

Prepping Department: PCB marking and component lead-forming operations, preparatory to manual insertion, comprise some of the operations performed in this department.

Automated Insertion: A number of numerically controlled machines insert a variety of components (DIPs, SIPs, VCD and axial lead) into PCBs. Each machine may only be used to insert one type of component. A sampling inspection procedure is carried out on assemblies before they leave the department and are routed to Manual Insertion.

Manual Insertion: The vast majority of boards require at least some manual loading of components. Seven workstations are devoted to this task.

Wave Solder: After a pre-solder inspection, assemblies are wave soldered on one of two machines. Post-solder inspection and touch-up operations follow. Also, components which cannot withstand the harsh conditions of the wave solder operation are installed on boards manually at this point.

NIT Test: A Nodal Impedance Test is used to identify assembly defects such as wrong or missing components. All boards in a lot are run through the test in "sort" mode -- a simple pass/fail test. Boards which pass this test are sent to the next operation in the test sequence; boards which fail are set aside. Periodically, the test operator will go into "debug" mode in which failed boards are diagnosed on the test apparatus, repaired and retested.

Burn-In: Boards are mounted on racks and placed in an environmental (high-temperature) stress chamber and cycled electrically for 24 hours in order to induce component "infant mortality."

Functional Test: This is the ultimate electrical test in which products are exercised to assure proper function. Each test station operates in "sort" and "debug" modes as was described above under NIT test. Here, however, defective boards may cycle through the test-repair-retest loop several times before all errors are identified and corrected.

Vendor: Often, the capacity of the plant will be augmented through the use of vendors. Services performed include assembly/wave solder and sometimes NIT test. All boards processed by vendors, however, must be functionally tested in-plant.

3. SIMULATION MODELLING TECHNIQUES

In order to obtain accurate and reliable answers to policy-related questions pertaining to a complex manufacturing system through computer simulation, an accurate and reliable model of the subject system is required. To achieve maximum impact on management, it was thought best to preserve in the model as many of the real-world characteristics of the system and its operation as possible. For these reasons, a stochastic modelling approach, in which key system properties such as product demand and production processing times are drawn at random from statistical distributions, yielded to a deterministic approach in which these traits were determined using existing records.

Associated with each circuit board type to be modelled was information concerning:

- 3 years of monthly product demand,
- production process routings,
- processing times for each assembly and test operation in the process routing,
- production leadtime, and
- expected test yields.

All of these data were organized in computer files to be used by the simulation model. The demand and leadtime data were used as input to other computer programs which generated time-phased order release schedules according to alternative order release and lot-sizing rules.

A network model of the production facility was conceptualized and translated first to the SLAM II graphical language, and subsequently to SLAM computer code. The scope of the computer simulation model spanned all assembly and test operations encountered by a board from the time it is released until the time it is completed and ready for shipment. The computer model required approximately 4000 lines of code (for a detailed account of the model and the project in general, see Shevell (1985)).

Entities travelling through the network model from one operation to the next represented production lots (or portions thereof). In SLAM, each entity flowing through a network has an associated attribute list. This list provides the modeller with a convenient means of storing information pertaining to the entity. In this case, relevant information includes process routing, operation times and test yields. To limit computer storage requirements for entities and their attribute lists, the attribute lists were limited to 14 entries per entity. SLAM discrete events were used extensively to draw data from files maintained external to the network, and insert the data into the appropriate place in the attribute list at appropriate times during the simulation.

SLAM discrete events are nothing more than user-written FORTRAN subroutines which are called from the network model whenever an entity arrives at a specified SLAM network node. In the simulation model, an entity representing a lot of boards would arrive at a node related to the start of a production

operation, and would have relevant information about that operation (e.g., processing time) inserted into its attribute list through the use of a discrete event. Network processing (e.g., delay) of the entity would proceed according to the information now accessible as an attribute of the entity.

In the model, entities have a dual nature: they represent production lots when flowing in the network from one operation to the next, but processing at machines or workstations is carried out on a board-by-board basis. The ability to model individual boards is especially important at test stations. There, boards either pass or fail the test. Boards which pass are routed to the next operation, while those that fail remain behind to be repaired and recirculated through the test station. Recirculation continues until the boards are defect-free. If board-by-board processing is important, why bother to model entities as lots at all? Work in process levels in the simulated factory approach 70,000 boards during the simulation. The computer memory necessary to hold 70,000 entities, their associated attribute lists, as well as the SLAM program code, exceeds the 4 megabytes of virtual storage available on the IBM 4341 computer used to run the simulation. A compromise which exploited the dual nature of the entity was found. The maximum number of entities existing in the network at one time would be equal to the total number of production lots in process (in the hundreds) plus the number of machines and workstations in the model multiplied by the maximum allowable lot size (80 x roughly 300 = 24,000), for a grand total of about 25,000 coexisting entities. This number could be accommodated.

The mechanism which allows for the dual nature (lot/board) of entities involves discrete events. As a lot-entity reaches a workstation, a discrete event subroutine is called which "explodes" the lot into a set of board-entities equal in number to the lot size (stored in the attribute list). These boards are queued and processed at the workstation. When processing on the lot's worth of boards is complete, the boards are reduced to a singular entity, once again representing the lot, and routed to the next operation.

An important factor to be investigated in the simulation study was the rule employed in choosing the next job (lot) to be processed at an operation. To model this, jobs arriving at a department were queued in a dispatch area to await processing. The factory as a whole thus resembles a series of pseudo-dynamic job shops as defined by Buzacott and Shanthikumar (1985). Here, each "mini-job shop" consists of the group of machines or workstations in the production department and the dispatch area. Scheduling the next job to be processed is controlled at the dispatch area. The special case for pseudo-dynamic job shops referred to by Buzacott and Shanthikumar applies here: while the dispatch area controls the priority assigned to waiting jobs, the jobs are released from the dispatch area (i.e., scheduled) only when a machine or workstation becomes available. This process is modelled by selecting the next job to be processed from among those waiting according to which lot-entity has the lowest value of a particular attribute compared to others in the queue. A discrete event is used to place either due date or processing time information into arriving entities' attribute lists. Thus, two alternative dispatch priority rules may be modelled in the simulation: Earliest Due Date and Shortest Processing Time. In the base case, the due date rule is used.

A final point of interest involves the modelling of shifts. In the real-world plant, most workstations operated over two 8-hour shifts. However, some workstations did not function during the second shift, while others were operated for three shifts. Also, provision for overtime had to be included in the model. To model shifts and overtime accurately, SLAM "PREEMPT" nodes were used at each operation so that the operations could be selectively stopped and started according to a schedule. PREEMPT nodes allow emanating activities to operate as long as an associated RESOURCE is available. When the RESOURCE is otherwise allocated, activity is suspended until the RESOURCE once more is made available. By carefully scheduling the allocation of RESOURCES, shift and overtime modelling was accomplished.

4. VERIFICATION AND VALIDATION

Model verification, or the "debugging of the logic and code of the computer [simulation] program" (Schruben, 1980), was accomplished through rigorous testing of each of the model's component modules using specially-developed input data and custom-designed reports. The test data were created so as to test each model component under every imaginable condition (naturally, further bugs were discovered when the model was subjected to the (unimaginable) conditions of production input data). Custom reports allowed the modeller to trace individual production orders as they progressed through the modelled factory. As each module was proven, it was integrated into the larger whole and retested as part of the overall system.

Model validation is usually defined to mean "substantiation that [the] computerized model within its domain of applicability possesses a satisfactory range of accuracy consistent with the intended applications of the model" (Schlesinger et al., 1979). Several validation techniques (after Sargent, 1983) were used in this project. Among them:

Face Validation: Plant management reviewed and approved logic diagrams for each model segment.

Event Validation: Model output was reviewed by management. Process flow times and inventory levels, for example, were found to be consistent with real-world records.

Internal Validation: The stochastic variability inherent in the model was

measured and shown to fall within the limits required so that statistical inference from the results was possible.

Comparison with Analytical Models: Output from certain model segments compared favourably to predictions obtained from analytical models of appropriate queueing systems.

Model validity was most convincingly demonstrated through Historical Data Validation. A graph of weekly production input and output versus time was produced during a simulation run of three years simulated duration. The major feature revealed in the graph (Figure 2) is a period of time over which there appears to be a severe capacity shortfall -- weekly output falls far behind and below weekly production input. Plant management remarked, upon viewing this graph, that the period of simulated capacity shortfall corresponded, when the simulated dates were mapped onto real-time, precisely to a period during which similar problems were encountered in the actual facility. Furthermore, the magnitude of the shortfall in terms of increased work in process inventories predicted by the model match real-world magnitudes. Finally, the machine centres identified as bottlenecks contributing to the simulated crisis were identified by managers as those that caused the problems in the historical situation.

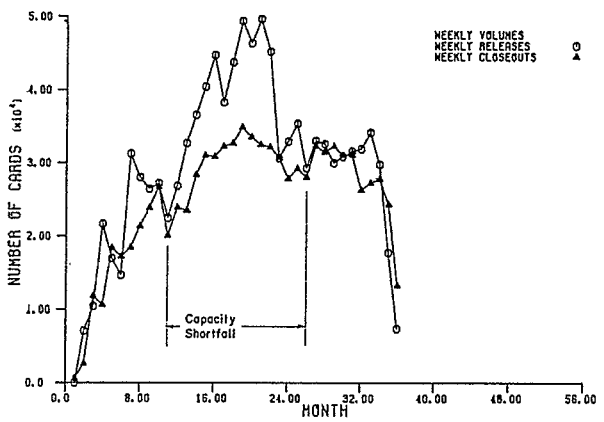

Figure 2: Simulated Production Capacity Shortfall

5. EXPERIMENT DESIGN

Through preliminary studies and a survey of plant management, a large list of potential issues was reduced to five factors which were to be studied using the simulation model. These were:

A. frequency of production order release,

B. dispatch priority rule used in assigning the next job to be processed in a department,

C. maximum allowable lot size,

D. hours of overtime worked per shift, and

E. product quality level.

The effects of these factors on production efficiency was measured in terms of:

1. percent of units completing processing behind schedule,

2. flow times of jobs through various departments and the systems as a whole, and

3. work in process levels in various departments and the system as a whole.

An experimental design was employed to measure both the effects of the five factors individually as well as how the factors interacted with each other. Each factor was assigned two possible levels, yielding a 2^5 full-factorial Hadamard matrix design. This design called for 32 simulation runs over which all possible combinations of factor high/low settings were accounted for. The design used 15 contrasts for estimating the main effects and 2-factor interactions, with 17 contrasts left over for estimating variance: all 3-factor and higher order interactions were assumed to be zero. This allowed for very precise statistical statements to be made about the effects of the factors acting alone and in combinations of two using a minimum number of simulation runs. Each simulation run covered 30 months of simulated time with a 4-month warm-up period.

Factor levels investigated were as follows: Production order release frequency was either WEEKLY or DAILY, as described previously; dispatch priority rule was either Earliest Departmental Due Date (EDDD) or Shortest Processing Time (SPT) in the department; maximum allowable lot size could either be SMALL (199 units) or LARGE (299 units); hours of overtime could be set at either NONE or 2 HOURS per shift; and quality levels were set at either the status quo level or 20% better than that. Quality was defined as being related to the first pass yield of products in the test operations. A 20% improvement in quality results in a 20% amelioration of each product's first pass yield in each test it undergoes. The possible factor level settings are summarized in Table 1.

Table 1: Factors Studied in the Experiments

Factor	Code	Description	-- Levels --	
A	POR	Production Order Release Frequency	Daily	Weekly
B	DISP	Dispatch Priority Rule	SPT	EDDD
C	LOT	Lot Size Threshold	100	150
D	HRS	Hours of Overtime Per Shift	0	2
E	QUAL	Quality Improvement Factor	20%	0%

Performance measure data for cycle time and work in process (WIP) levels were collected for the auto insertion department (the prototypical assembly department), NIT test (a bottleneck department with characteristically low first pass yield statistics), functional test (where a high degree of recirculation results because defects are not often identified and fixed on the first attempt at debug and repair), and the system as a whole. Percent Behind Schedule results were collected only for boards completing processing in the system as a whole.

6. RESULTS AND DISCUSSION

Experimental results from the 32 simulution runs were analyzed using linear regression. Residual analysis led to our use of regression models with a multiplicative functional form in which the independent variables were transformed exponentially. When natural logarithms are taken on both sides, the resulting models are linear and additive. The following models were fit to the data to probe the significance of the main effects:

$$\ln(\text{dep var}) = \beta_0 + \beta_1.\text{POR} + \beta_2.\text{DISP} + \beta_3.\text{LOT} + \beta_4.\text{HRS} + \beta_5.\text{QUAL} + \ln \epsilon$$

Table 2 shows coefficient estimates obtained from these models. Only coefficients significant at $\alpha = 0.05$ are included. Augmented models were used to assess two-factor interactions.

Table 2: Coefficient Estimates for Significant Main Effects

	Factors and Coefficient Estimators					
Dependent Variables:	Intercept $\hat{\beta}_0$	POR $\hat{\beta}_1$	DISP $\hat{\beta}_2$	LOT $\hat{\beta}_3$	HRS $\hat{\beta}_4$	QUAL $\hat{\beta}_5$
% Behind Schedule	3.0512	0.3077	0.1207		-0.4033	0.1205
System WIP	10.3530	-0.0034	0.0194	0.0105	-0.1775	0.1438
System Cycle Time	5.7108		0.0722	0.0128	-0.1982	0.1301
Auto Insert WIP	5.8187		-0.0034	0.0474	-0.0908	
NIT WIP	8.2407		0.0929		-0.9326	0.5618
Funct. Test WIP	9.0275	-0.0063		0.0165	-0.1260	0.2051
Auto Insert Cycle	3.0187			0.0538	-0.0649	
NIT Cycle Time	4.6547	-0.0326	0.0706		-0.9045	0.5525
Funct. Test Cycle	3.7591		0.4023	0.0467	-0.1119	0.0982

The regression models were used to construct 95% confidence intervals for the performance measures under various combinations of factor level settings. Using these results, "ideal" policies, which yielded the best performance for each measure, were obtained. Since higher quality levels are modelled without taking into account the potentially higher price to be paid in obtaining them (e.g., more inspection in assembly, etc.), it is not surprising that performance on all measures was found to be highest when high quality levels were coupled with 2 hours of overtime per shift. Unfortunately, quality levels are difficult to alter in short order, and management is reluctant to authorize overtime if better performance may be obtained by other means. Therefore, let us assume that both HOURS worked and QUALITY levels remain at status quo settings, and investigate which settings of the other factors yield highest performance.

Table 3 shows the ideal factor level settings recommended by the model to achieve high performance for the various measures with HRS and QUAL at status quo levels. Only significant factors are shown.

Table 3: Factor Level Settings Recommended by the Model (with HRS and QUAL at status quo levels)

Measure	Factor				
	POR	DISP	LOT	HRS	QUAL
Percent Behind Schedule	DAILY	SPT	*	16	LOW
System WIP	WEEKLY	SPT	SMALL	16	LOW
System Cycle Time	*	SPT	SMALL	16	LOW
Auto Insert WIP	DAILY	*	SMALL	16	LOW
NIT WIP	*	SPT	*	16	LOW
Functional Test WIP	WEEKLY	*	SMALL	16	LOW
Auto Insert Cycle Time	DAILY	*	SMALL	16	LOW
NIT Cycle Time	WEEKLY	SPT	*	16	LOW
Functional Test Cycle Time	*	SPT	SMALL	16	LOW

* Not Significant at $\alpha = 0.05$

What is the ideal setting of factors for the manufacturing facility? Consider the 16-hour workday and base case quality levels as given. Of the remaining three factors, the easiest to deal with is lot size: in all cases performance improves when smaller lots are used. Consider next the frequency of production order release, factor POR. Here there is a conflict. The Percent Behind Schedule and Auto Insert department measures are best under a DAILY releasing scenario, while the other measures for which POR is significant fare better under the WEEKLY releasing scheme. More detailed examination of the results, however, made the tradeoff decision rather straightforward. If DAILY release is chosen the measures for functional test and system WIP and NIT Cycle Time suffer by 2%, 1% and 6%, respectively. On the other hand, the "wrong" (WEEKLY) choice for POR with respect to Percent Behind Schedule translates into a 46% slide in that performance measure. On balance, then, DAILY production order release is prescribed.

Finally, a choice of dispatch priority rule must be made. The evidence in Table 3 suggests that the SPT rule would be superior to EDDD in all cases. One must be cautious in making this assertion, however. When HRS = 20 (vs. 16) and QUALITY levels are 20% higher than the status quo, the system WIP and Percent Behind Schedule measures strongly favour the EDDD rule over SPT. Further, there is a significant 2-factor interaction between DISP and HRS for the above two performance measures. The 2-factor interaction was interpreted as suggesting that SPT outperforms EDDD when HRS = 16, but that either rule may be used without adverse effect when 2 hours of overtime are worked per shift. These two additional insights intimate that EDDD may be preferable where there is an excess of capacity, at least insofar as the

Percent Behind Schedule and system WIP measures are concerned; SPT seems to be the rule of choice when capacity is at a premium. This idea is reinforced when NIT WIP results were examined under different NIT department loading conditions. When the department was loaded at or above capacity, SPT was preferred; when the department was lightly loaded, the DISP factor was not even significant. Naturally, SPT would be the rule of choice when cycle time measures are important.

Two final points should be noted: First, the dispatch priority rule need not be employed uniformly throughout the plant. It would be possible to use EDDD in areas where sufficient capacity exists, and SPT in more heavily-loaded production departments. Second, since the SPT calculation is based partly on lot size, there is the danger that a relatively large lot made up of boards requiring long processing times may never be selected for processing! One practical method for avoiding this situation would be to use a 2-class priority scheme. Class A would consist of those large jobs of the type described above. They would be processed on either a first-come-first-served basis or EDDD with high priority. The remaining Class B jobs would be selected from among those waiting using an SPT rule.

7. CONCLUSIONS

The research reported in this paper yielded two main results. First, the design and implementation of the simulation model and computer program was an important part of the research. It involved studying the manufacturing system in great detail, and then creating an abstract representation of it. Creating and fine-tuning the simulation program provided opportunities for learning even more about the manufacturing system, and how to model it accurately and efficiently. The result of these efforts is a detailed, accurate and reliable tool with which one can estimate the effects of changing operating conditions on the performance of the manufacturing system.

Second, there are the results of the analysis of the simulation experiments. Several factors were found to have a major impact on the performance of the manufacturing system. Also, some factors were found to interact in a significant way. The analysis showed that quality levels and the number of hours worked per day had the greatest influence on system performance. These results confirmed what had been expected. The influence of the other factors could not be predicted in advance, and the experiments provided valuable insights into policies that could be pursued in order to push system performance toward optimum levels. Specifically, small lots, daily production order release schedules, and an appropriate combination of earliest due date and shortest processing time dispatching priority rules produced the best results in the simulation experiments.

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