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VIRTUAL SEMICONDUCTOR FABRICATION: IMPACT OF WITHIN-WAFER VARIATIONS ON YIELD AND PERFORMANCE

Sumant Sarkar[1], Brett Lowe[1], and Benjamin Vincent[2]

[1]Lam Research, Hillsboro, OR, USA
[2]Lam Research, Paris, France

ABSTRACT

The semiconductor industry aims to enhance device performance while maintaining a high yield. Managing variations in process steps is a challenge, traditionally addressed through physical silicon experimentation. This study developed a virtual fabrication model of a FinFET transistor to analyze the impact of process variations, such as etch and deposition steps, on key transistor parameters like threshold voltage (Vth), Drain-Induced Barrier Lowering (DIBL), and subthreshold swing (SS). Analysis of within-wafer variations in spacer nitride thickness revealed significant variability, affecting Vth and yielding 66.7%. Adjusting the nominal spacer nitride deposition thickness and controlling deviations improved yield, confirmed by Monte Carlo simulations. Three process recipes with different deposition thickness distributions were tested, with the "donut" region recipe achieving the highest yield (94.8%) and smallest Vth standard deviation. Additionally, combined variations in spacer nitride deposition and epitaxial SiC growth thickness were analyzed, demonstrating the model's capability to predict and optimize multiple process recipes.

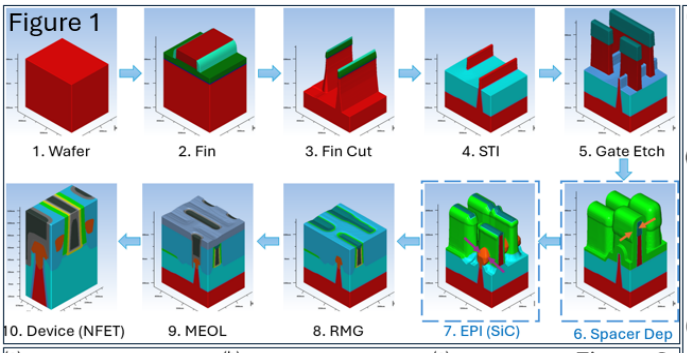
1 INTRODUCTION

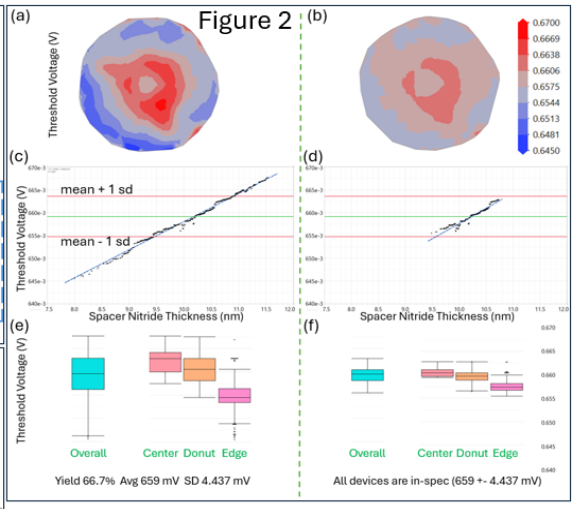
Within-wafer variations in device and die characteristics have long been a critical issue in semiconductor fabrication. These die-to-die and device-to-device variations can significantly impact yield (Smith et al. 1999). To mitigate these variations, advancements in process improvements and chamber design are essential. Virtual fabrication and modeling methods have proven beneficial in this regard, facilitating pathfinding to enhance lithography, etch, and deposition processes. Despite varying degrees of success, there remains a need for virtual fabrication methods capable of measuring wafer-wide yield and variations. Such methods would enable a comprehensive assessment of the impact of process improvements. Additionally, they would allow for the selection of optimal process improvement candidates based on overall yield and within-wafer uniformity.

2 METHODS AND RESULTS

A virtual model for the fabrication process of a 14nm FinFET transistor was developed (Figure 1) using Lam Research's SEMulator3D® (Hargrove et al. 2023). This model was employed to predict key device parameters: threshold voltage (Vth), Subthreshold swing (SS), and Drain Induced Barrier Lowering (DIBL). A Wafer-Wide (WiW) map exhibiting low WiW uniformity of deposition thickness was analyzed. The virtual device performance data was measured, and the WiW uniformity was evaluated using a Monte Carlo simulation consisting of 1000 runs (Figure 2). The map with this low WiW uniformity highlighted significant variations in device characteristics across the wafer, indicating the need for process adjustments. Based on a linear regression model (Figure 2-c), the optimal value for the deposition thickness was obtained. Also, the maximum allowed variation allowed in deposition thickness that would ensure all devices to be in-spec (within 1 σ from mean) was calculated. Having obtained the new optimal value of deposition thickness and the maximum variation allowed, a new wafer map was generated. The Monte Carlo

simulation was repeated for this map and the variations in transistor characteristics were investigated (Figure 2). Three process improvement recipes were proposed which have the identical (10%) maximum variations in deposition thickness. However, their gaussian distribution across the wafer regions were different. Recipe 1 had a higher thickness at the center of the wafer. Recipe 2 had a higher thickness at the edge of the wafer. Finally, recipe 3 had a higher thickness in the middle (donut) region of the wafer. The Monte Carlo simulation was repeated for these and the variations in transistor characteristics were investigated. The recipe with the least amount of variation and the highest yield was identified (Figure 3). Next, both Spacer Nitride thickness and epitaxial SiC growth thickness were varied (using recipe 3 and 2 respectively) with a maximum of variation of 12%. The resultant variations in device characteristics were analyzed. Linear regression equations that incorporate both Nitride thickness and SiC growth thickness were obtained.





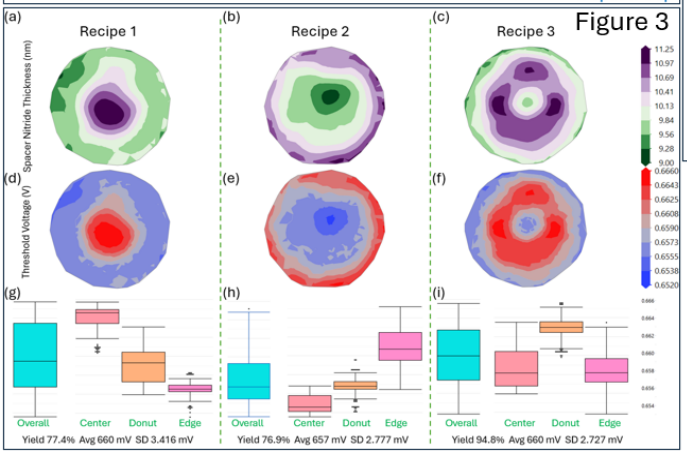


Figure 1: Virtual fabrication model of a (14nm FinFET) transistor showing the key process steps. Steps #6 (Spacer Nitride Deposition) and #7 (Epitaxial SiC growth) are the subject of this study.
Figure 2: (a-b) Variations in transistor threshold voltage across the wafer, illustrating high variations and low uniformity. (c-f) Variations in transistor threshold voltage across the wafer with lower variations, demonstrating improved uniformity.
Figure 3: Spacer nitride thickness variations across the wafer for (a,d) Recipe 1, which has higher thickness at the center. (b,e) Recipe 2, which has higher thickness at the edge. (c,f) Recipe 3, which has higher thickness in the middle (donut region). (g-i) Recipe 3 demonstrates the smallest standard deviation and highest yield among the three recipes.

3 CONCLUSIONS

In this study, we addressed the critical issue of within-wafer (WiW) variations in device and die characteristics during semiconductor fabrication. By leveraging Lam Research's SEMulator3D® to create a virtual model, we were able to predict key device parameters and evaluate WiW uniformity. Using a linear regression model, we arrived at the thickness and maximum variation allowed that would ensure that all devices are in-spec. The scheme allowed comparison multiple candidates of process recipe improvements. This method also allows us to assess the combined impact of WiW variations in multiple process steps

REFERENCES

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