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# DIGITAL TWIN-BASED REINFORCEMENT LEARNING FOR OPTIMIZATION OF LOT MERGING EFFICIENCY IN FINAL TEST OPERATIONS OF SEMICONDUCTOR PRODUCTIONS

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## ABSTRACT

The final test operation in semiconductor production, which verifies the electrical functionality of packaged chips, demands highly responsive logistics and equipment control strategies to meet delivery, ensure quality, and accommodate urgent requests. In complex production environments involving diverse products and many different process constraints, optimizing both lot merging efficiency and equipment utilization becomes more and more critical. This paper presents an integrated framework that combines digital twin simulation with deep reinforcement learning, a Rainbow DQN agent, to enhance success rates of lot merging and improve throughput. While preserving the existing MES-driven dispatch logic, the framework introduces a learning-based policy that leverages equipment characteristics—particularly the constraint that higher-parallelism tools have narrower merging time windows. The agent learns to dynamically adjust lot-to-tool assignments, reducing resource waste and idle time, while supporting more efficient and predictable production scheduling.

## 1 INTRODUCTION

In semiconductor final test operations, failed devices undergo 'Retest' after an initial 'Main Test'. If lots of the same product arrive within a limited window, lot merging can occur, reducing redundant operations and improving equipment efficiency. As shown in Figure 1 (Left), merging-enabled logistics streamline the process compared to conventional scenarios. However, a critical constraint in enabling lot merging lies in the merging window—the limited period during which additional lots must arrive before the tool becomes fully loaded. Once the equipment begins processing and reaches its full capacity, no further merging is possible. This constraint becomes more severe for tools with high parallel test capacity. Because these tools can test more devices simultaneously, they complete the 'Main Test' more quickly and become fully loaded faster, effectively narrowing the merging window. As a result, the probability of successful lot merging decreases even though these tools are designed for high throughput. Traditional dispatch systems, which prioritize due dates or WIP levels without considering lot merging opportunities, fail to synchronize lot flows with tool-level merging conditions. As illustrated in Figure 1 (Right), merging rates sharply decline as parallel test capacity increases, highlighting the inefficiency of conventional WIP management.

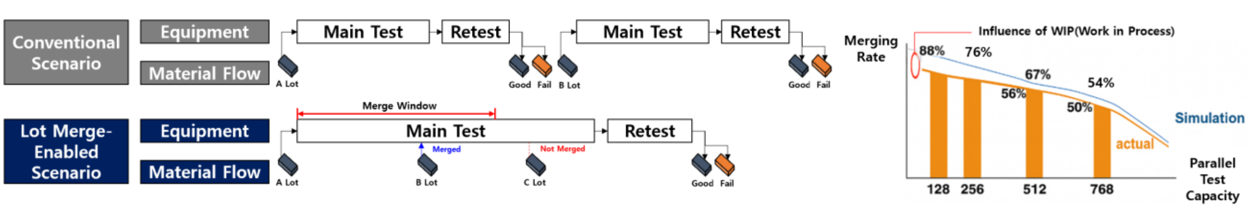


Figure 1: (Left) Test flow comparison with and without merging. (Right) Example of Merging rate.

To address this, we propose a digital twin-based reinforcement learning framework that dynamically controls WIP distribution across equipment. By optimizing lot dispatching in consideration of merge windows and parallel test capacity characteristics, the framework increases the chance of successful *lot merging* and ultimately enhances unit-per-equipment-hour (UPEH) performance.

## 2 FRAMEWORK OVERVIEW

The proposed framework integrates a digital twin simulation model with a reinforcement learning agent to optimize lot dispatching in final test operations. The digital twin, by *Siemens Plant Simulation*, reflects real-time states from the manufacturing database—including equipment parallel test capacity status, logistics scheduling, and WIP buffers—and simulates the production environment accordingly. The RL agent, trained in *Python*, receives state and reward feedback based on UPEH improvement and production target achievement. Merge-related constraints are encoded in both simulation logic and reward calculation, enabling the agent to learn dispatch policies that improve lot merging efficiency, particularly for high-parallel test capacity tools, ensuring compatibility with existing MES operations.

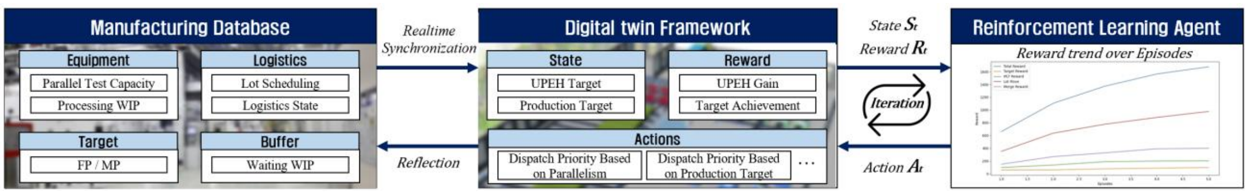


Figure 2: Overview of the digital twin-based reinforcement learning framework.

## 3 SYSTEM IMPLEMENTATION

In the simulation layer, lot merging success is determined by whether lots of the same product arrive within a tool-specific mergeable time window. Upon a successful lot merging, the tool's processing time is reduced based on predefined efficiency parameters that reflect its parallel test capacity. If merging fails, the standard processing time is applied. The reinforcement learning agent prioritizes lots for each tool based on real-time WIP conditions and parallel test capacity. Tools are sorted accordingly, and lots are allocated to favor mergeable combinations while ensuring load balance. Finally, the dispatch policy is refined through iterative learning episodes, with feedback derived from key performance indicators such as lot merging rate, UPEH, lot movement, and target achievement.

## 4 EXPERIMENTS AND CONCLUSION

The proposed framework was validated in a simulated final test environment with various tool configurations. The reinforcement learning-based dispatch policy consistently improved lot merging-related rewards throughout training episodes, and led to overall performance gains in UPEH, lot movement, and target achievement. By augmenting traditional MES logic with a merging-aware learning agent, the system effectively reduced inefficiencies in retest operations and improved utilization of tools with high parallel test capacity. Future work will explore extending the approach to more diverse product mixes, forecasting merge windows using time-series models, and integrating long-term capacity planning strategies. These results highlight the framework's potential as a scalable and practical solution for intelligent scheduling in final test operations of semiconductor productions.

## REFERENCES

Lu, Shaojun, et al. "Scheduling of memory chips for final testing on parallel machines considering power constraints and deteriorating effects." International Journal of Production Economics 278 (2024): 109413.

K. Agalianos, S. T. Ponis, 2021. "Discrete Event Simulation and Digital Twins: Review and Challenges for Logistics" Procedia Manufacturing 51 (2020) 1636–1641

J Liu, X Cao, H Zhou. 2021. "A digital twin-driven approach towards traceability and dynamic control for processing quality" Advanced Engineering Informatics 50 (2021) 101395

Ahmed Zainul Abideen, "Digital Twin Integrated Reinforced Learning in Supply Chain and Logistics". Logistics, 2021