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COMBINED DEVS MULTIRESOLUTION SIMULATION AND MODEL CHECKING

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ABSTRACT

We propose using Multiresolution Modeling (MRM) for system level design of networked software systems. This methodology aids in creating a family of models at different levels of complexity. We have developed an MRM framework to support hierarchical modeling as exemplified for Network-on-Chip (NoC) systems, as exemplar of network systems, with support for both validation and verification. Throughout the design phase, fine-grain models are created using their coarse-grain counterparts. Each model can be validated using discrete-event simulation and verified using model checking. We propose Constrained-DEVS, a variant of the Discrete Event System Specification (DEVS) formalism, which supports model checking in addition to DEVS's discrete-event simulation capability. Appropriate execution protocols for mixed V&V (validation and verification) are proposed. This leads to an MRM framework enabling both simulation and model checking. This framework is realized through extending the DEVS-Suite simulator and its applicability demonstrated for exemplar NoC models.

1 APPROACH

While NoC models are categorized in four abstraction levels, it is challenging to define relationships between two models at different abstraction levels. One method to clearly related such models is using the concept of resolution. Resolution is defined to have four dimensions: Process, Object, Time, and Space; modeling behavioral, structural, temporal, and physical aspects of the system respectively. We add Data as another dimension to resolution. This is necessary for systems in which the communication of data is an integral part of the model. In a Network-on-Chip system, data exchange is by itself a part to be modeled, validated, and verified. Thus, data is considered to be represented at varying resolutions within each of the abstraction levels. One may use these five dimensions to distinguish models of NoC from one another. To develop NoC models, the modeler has spatial resolution (such as including VIAs and layers in the model), object resolution (hierarchies and the components included), process resolution (details included in the behavior of the model), temporal resolution (granularity of time), and data resolution (units of data being communicated and the levels of detail in each unit) at his/her disposal at various abstractions. Each model may serve a specific purpose in the V&V process.

During system design, various models of the system are developed. Dynamical models are often necessary to be evaluated using both verification and validation techniques throughout incremental design stages. Designers use both validation and verification techniques in order to achieve some degree of assurance that the model is an accurate representation of a reference model or system. DEVS is well suited for validation through simulation as supported in tools such as DEVS-Suite (ACIMS 2017); however, DEVS is not suitable for model checking because of the continuity of time and boundless state variables. To counter these fundamental characteristics, we have introduced Constrained-DEVS (Gholami and Sarjoughian 2017) which makes model checking possible by 1) introducing lower/upper bounds and

discretizing state variables, 2) restricting the number of input events, and 3) forcing the number of internal/external transitions to be finite within any finite period of time. A state exploration protocol is designed and DEVS-Suite is extended to support realizing Constrained-DEVS models and model checking them against prescribed properties. We kept the simulation capability of DEVS-Suite intact; therefore, Constrained-DEVS models are multi-purposed as they can be used for both simulation and model checking. It is worth noting that state exploration protocol in DEVS-Suite incorporates existing simulation protocol.

Constrained-DEVS and its realization in DEVS-Suite provide new capabilities for V&V. One is a powerful property expression method. As mentioned Constrained-DEVS models can be verified against certain properties. These properties are defined and checked by transducer models. The Experimental Frame (EF) is another aspect of DEVS which is used here in both simulation and model checking. The transducer constructs the state reachability graph based upon the reachable state set explored by the model checking protocol. This graph is then used by the transducer to check for various types of properties. Using EF, complex properties (such as performance-related properties) can be expressed (not supported in CTL, LTL, and TCTL (Lanotte, Maggiolo-Schettini and Troina 2005)) and verified by the verification engine.

Another key capability of the Constrained-DEVS and DEVS-Suite pair is *Selective State Exploration*. While model checking, one can easily include/exclude state variables of a model from the exploration algorithm. This way, modeler can control the number of state variables and thus restricting the exploration of the state space. In addition, based on the properties under investigation, some state variables may not be necessary to be included in the state space search. Use of state variables can be managed by simply turning them on or off . This is in contrast with other approaches (e.g., Petri nets and Timed Automata) in which a model's state space once created cannot be reconfigured.

2 SUMMARY

Overall, our contribution (multiresolution models of NoC and the introduction of Constrained-DEVS) and extended DEVS-Suite framework enables creating, verifying, and validating models of a system at different resolutions. The validation (via simulation) and verification (via model checking) are both managed by experimental frame. While state explosion remains challenging for models such as NoC, in this framework, users can control unbounded model complexity through model resolutions and selective state explorations. This DEVS-based hybrid framework eliminates the need to transform models developed for simulation to representations that can be model checked.

While high-level formal modeling is rewarding during the design of complex hardware systems, Hardware Description Languages (HDL), for low-level modeling and synthesis, are still necessary steps to have actual chips. MRM is not limited to any formal modeling approach. This research can lead to applying MRM for HDLs such as Register-Transfer Level (RTL) DEVS models. While formal validation and verification on hardware-level DEVS models is important for evaluating design correctness and satisfaction of performance properties, automatic transformation of DEVS models (from the existing hardware-level model library) to HDL facilitates synthesis and workload testing on chip implementation.

REFERENCES

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