Proceedings of the 2017 Winter Simulation Conference
W. K. V. Chan, A. D'Ambrogio, G. Zacharewicz, N. Mustafee, G. Wainer, and E. Page, eds.

ANALYZING DIFFERENT DISPATCHING POLICIES FOR PROBABILITY ESTIMATION IN TIME CONSTRAINT TUNNELS IN SEMICONDUCTOR MANUFACTURING

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ABSTRACT

In semiconductor manufacturing, new technologies impose more and more time constraints in product routes, i.e. a maximum time between two (often non-consecutive) operations. The management of Time Constraint Tunnels(TCTs, combining multiple time constraints) in high-mix facilities is becoming more and more challenging. This paper first recalls an approach for estimating the probability that a lot at the entrance of a TCT will leave the TCT on time. This approach relies on a list scheduling algorithm using a dispatching policy with random components. Three dispatching policies are presented. Computational experiments on industrial data comparing these policies are discussed. Perspectives are drawn to extend the approach and support decision making.

1 PROBLEM DESCRIPTION

In view of an already complex context of high product mixes and low volume products, the management of TCTs has become increasingly challenging. To address these challenges, we have built upon a graph based probability estimation approach mixing simulation and list scheduling, and improved the approach by introducing an alternate scheduling policy. This policy aims at replicating the ubiquitous dispatching rules existing in the fab and better fits the industrial reality. Hence, the contribution of this article is twofold: (i) To provide an original approach that can support TCT management, and (ii) To introduce a new more realistic scheduling policy. In order to emphasize the soundness of the proposed approach, extensive numerical experiments have been conducted based on industrial instances. The initial algorithm can be succinctly described as follows: A given set of lots and tools constitutes a time constraint tunnel and its traffic at a given point in time is modeled through a disjunctive graph representation. We introduce a single fictive lot at the first step of its set of time constraints. We then successively generate feasible schedules for all the lots including the fictive lot based on a random dispatching policy. For each schedule, we check if the fictive lot has exceeded each time constraint. Finally, the success probability is calculated by dividing the number of successful iterations by the total amount of iterations.

2 DISPATCHING POLICIES

The initial policy being a pure random selection of the lots waiting in front of a machine, it does not accurately describe the actual behavior of lots in the fab and thus it was decided to enhance this policy. In semiconductor fabs, dispatching rules are extensively used because of their relative simplicity and ease of implementation, yet they bring concrete improvements to the product flow. Our goal is to replicate these dispatching rules into the algorithm. The most common dispatching rule is known as *standard dispatching rule*. It is a priority based rule, where each lot is ranked based on a given weight, so that the lot with the largest weight will always be processed first. This weight depends on a base priority factor and a number of other factors, namely: Whether the lot is entering a time constraint or not, the lot's due date, etc. More importantly, the weight increases with the lot's current waiting time at the operation. We strive to replicate

978-1-5386-3428-8/17/$31.00 ©2017 IEEE

this dispatching rule into the probability estimation algorithm. In order not to make the dispatching policy entirely deterministic and so that the law of large numbers still applies, we modify the policy by adopting a uniform distribution based selection of lots according to their calculated weights. The deterministic alternative would be to always select the lot with the largest weight.

3 EXPERIMENTAL RESULTS

The comparative analysis between both policies shows that the priority based heuristic is more time consuming (see Table 1) but provides a more accurate modeling in terms of translating what is reality happening in the fab, and thus provides a more accurate predictive model. However, in some ”easy” cases such as when the fictive lot has no chance of coming out on time or is sure to come out on time, both heuristics provide the same information and the random policy could be used. Both heuristics takes less than five minutes to converge according to a dynamically set criterion, which was a threshold set as an industrial requisite. The convergence criterion is also described in the full paper (Lima, Borodin, Dauzère-Pérès, and Vialletelle 2017).

Inst.		TCT 1			TCT 2			TCT 3			TCT 4			TCT 5		
		RAND	PIT	WAIT	RAND	PIT	WAIT	RAND	PIT	WAIT	RAND	PIT	WAIT	RAND	PIT	WAIT
3	IT Count	N/A	N/A	N/A	164	250	190	157	174	139	60	100	110	291	60	60
	CPU(sec.)	N/A	N/A	N/A	15	111	88	17	94	78	5	39	43	23	22	22
4	Iterations	161	120	109	N/A	N/A	N/A	200	100	263	N/A	N/A	N/A	60	212	231
	CPU(sec.)	1	5	4	N/A	N/A	N/A	16	37	98	N/A	N/A	N/A	6	96	11
8	Iterations	329	110	60	259	60	289	166	226	60	60	60	99	149	60	181
	CPU(sec.)	9	14	9	38	42	212	26	154	43	6	28	48	18	30	92
9	Iterations	N/A	N/A	N/A	N/A	N/A	N/A	278	60	149	222	60	60	60	120	60
	CPU(sec.)	N/A	N/A	N/A	N/A	N/A	N/A	60	66	163	45	54	56	8	67	37
10	Iterations	60	60	60	247	388	327	187	248	110	299	119	60	221	60	159
	CPU(sec.)	6	28	24	60	446	400	53	325	154	73	132	69	44	49	136
11	Iterations	N/A	N/A	N/A	209	109	301	171	60	100	180	60	149	255	60	277
	CPU(sec.)	N/A	N/A	N/A	42	118	338	5	8	13	32	57	144	35	40	185

Table 1: Number of iterations and computational times for all TCTs and instances

4 CONCLUSION

Future work will be dedicated to improving and expanding the decision support potential of the proposed probability estimation approach, by applying more thorough statistical analysis tools, in order to refine the convergence criterion, and to more closely assess algorithm parameters. The ultimate goal being to support decisions for the management of TCTs, we intend to enhance and extend the approach to derive valuable managerial insights, such as **(i)** Cycle time improvement, **(ii)** Detection of root causes of TC violations, etc.

REFERENCES

Lima, A., V. Borodin, S. Dauzère-Pérès, and P. Vialletelle. 2017. “Scheduling Jobs with Time Constraints between Consecutive Process Steps in Semiconductor Manufacturing”. In *Proceedings of the 2017 Winter Simulation Conference*, edited by W. K. V. Chan, A. DAmbrogio, G. Zacharewicz, N. Mustafee, G. Wainer, and E. Page, (to be published): Piscataway, New Jersey: Institute of Electrical and Electronics Engineers, Inc.