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A FRAMEWORK FOR EFFECTIVE SHOP FLOOR CONTROL IN WAFER FABS

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ABSTRACT

In order to gain a competitive position within industry, in semiconductor fabs enormous efforts have been spent in developing different kinds of operational control strategies relating to work-in-process (WIP) and due date. This paper presents a framework to deal with shop floor control problems regarding WIP balance and due date control. The framework comprises four key components that are (1) Global and local rules; (2) Target WIP estimation; (3) WIP imbalance monitor and detection; (4) WIP imbalance calibration. These four components clearly focus on their own specific tasks and support each other, in such a way that we can manage to: (1) Improve efficiency and productivity such as achieving low WIP and cycle time while keeping good on-time delivery; (2) Enhance intelligence of automated manufacturing such as reducing WIP variability and smoothing material flow via automated WIP imbalance monitor and correction.

1 INTRODUCTION

For traditional wafer fabrication facilities (wafer fabs) like mass production, work-in-process (WIP) is the main concern in shop floor control since it has a major influence on overall manufacturing costs. In general, WIP oriented rules (Folwer et al. 2002) are utilized to control the flow of lots to achieve balanced WIP to reduce variability, thus achieving cycle time reduction that brings significant economic benefit. As many wafer fabs move from mass production to mass customization to satisfy customers. Due date becomes another critical factor and due date oriented rules (Keskinocak and Tayur 2004) are applied to achieve on-time delivery in these fabs. The first challenge arising in these fabs is the conflicting goal between WIP oriented and due date oriented rules, as they reduce the weight of counterpart (Zhou 2014). It turns out that they are insufficient in today's advanced wafer fabs where both targets - low WIP level and good due date performance - are desired simultaneously.

Another challenge to shop floor control is the presented production variations, e.g., unpredictable machine breakdowns, batch processing, setup requirements and so on. These variations might give rise to WIP imbalance that can result in excessive WIP in some operations or work-centers (Yeh et al. 2008) or WIP bubbles and fluctuations (Dabbas and Fowler 2003, Zhou and Rose 2012b). This WIP imbalance phenomenon, which cannot be easily handled by traditional WIP oriented or due date oriented rules, has great impact on the material flow. In particular, it brings frequent and serious fluctuations to the WIP evolution curve, which imposes a huge challenge to accurate WIP and cycle time forecasts, as well as reliable due date commitments. In practice, WIP control and tracking mechanisms like WIP exception management (Guo et al. 2007), WIP position analysis (Zhou and Rose 2012b) and automated WIP flow management (Duemmler and Wohlleben 2012) are ways to reduce the harm of WIP imbalance and achieve operational targets.

In this paper, we present a framework focusing on developing different operational control strategies to deal with the shop floor control problems mentioned above. The goals are to: (1) Set up different dispatching rules to achieve balanced WIP or good due date performance respectively, or achieve both targets simultaneously; (2) Smooth material flows and reduce WIP fluctuations by means of WIP imbalance detection and correction.

This paper is organized as follows: Firstly we describe the major functions and tasks of each component in detail and explain how these components cooperate to achieve the overall goals; Secondly, we present the performance of a simulation model under the control of this framework; Finally, we conclude this paper by summarizing the finding from the simulation results and provide future research questions

2 A FRAMEWORK TO CONTROL WAFER FABS

The framework presented by this paper consists of four main components that are depicted in Figure 1. They are: (1) Global and local rules; (2) Target WIP estimation; (3) WIP imbalance monitor and detection; (4) WIP imbalance calibration. We will elaborate these four components in the following sections.

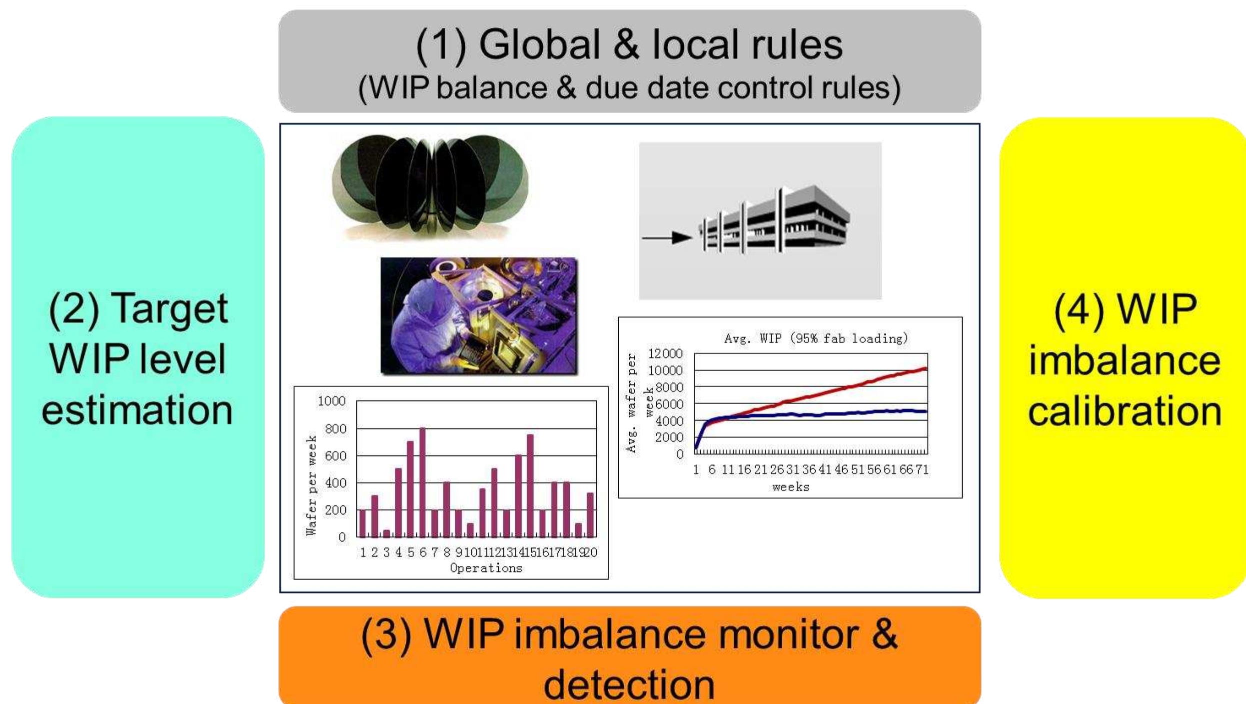


Figure 1: Four main components in the framework.

2.1 Global and Local Rules

The first component 'global and local rules' is the brain of this framework. It focuses on controlling the material flow through wafer fabs based on specified targets like WIP and due date. Thus, there are three categories of rules - WIP balance rules, due date control rules and WIP balance combining with due date control rules which are listed in Table 1.

When the operational target is WIP oriented, we can utilize WIP balance rules in this component. The WIP balance rules can be classified into operation oriented like minimum inventory variability scheduling (MIVS) (Li et al. 1996), line balance algorithm (LB) (Dabbas and Fowler 2003) and work-center oriented like balanced machine workload (BMW) (Ham and Fowler 2007) on the basis of different viewpoints of

WIP flow. We also develop four work-center oriented rules which are bottleneck oriented (Zhou and Rose 2009), WIP control table (WIPCT) (Zhou and Rose 2010), workload indicator (Zhou 2014) and minimum workload variability scheduling (MWVS) (Zhou 2014), for the reason we believe that managing WIP flow from the work-center viewpoint has more potential benefits than the operation viewpoint. We can incorporate local constraints like setup, batch and machine breakdown into decision making. On one hand, some rules can perform as global rules as they can avoid congestion and starvation in operation/work-center. As a result, they can reduce WIP variability for the whole fabs and achieve cycle time reductions. On the other hand, some rules can perform as local rules targeting on local optimization for some specified work-center, i.e., reducing variability of incoming and outgoing WIP flow of a bottleneck work-center to ensure high utilization and throughput.

Table 1: Global and local rules.

<table>
<tr><th colspan="3" rowspan="2">Dispatching rule</th><th colspan="2">Target</th></tr>
<tr><th>Global</th><th>Local</th></tr>
<tr><td rowspan="2">WIP balance</td><td>Operation oriented</td><td>MIVS, LB</td><td rowspan="2">• Fast lot movement;
• Reduce WIP variability;
• Reduce WIP and cycle time.</td><td rowspan="2">• Increase utilization and throughput for some specified work-centers.</td></tr>
<tr><td>Work-center oriented</td><td>BMW,
Bottleneck oriented,
WIP control table,
Workload indicator,
Minimum workload variability scheduling</td></tr>
<tr><td colspan="2">Due date control</td><td>EDD, ODD, A/OPN, LST, LOST, S/OPN, CR, OCR, MDD, MOD,
Modified MOD</td><td>• Well-paced lot movement;
• Increase on-time delivery;
• Reduce tardiness.</td><td>• Reduce cycle time variance for some specified manufacturing stages.</td></tr>
<tr><td colspan="2">WIP balance + due date control</td><td>**Matrix Table**,
Modified infineon global rule,
WIP control table combining with ODD</td><td>• Achieve low WIP level and cycle time, high on-time delivery simultaneously.</td><td></td></tr>
</table>

When due date performance is desired, some classical due date control rules (Baker and Trietsch 2009) can be found here, e.g., earliest due date (EDD), operation due date (ODD), allowance per operation (A/OPN), least slack time (LST), least operation slack time (LOST), slack per operation (S/OPN), critical ratio (CR), operation critical ratio (OCR), modified due date (MDD), modified operation due date (MOD). We also develop modified MOD (Zhou and Rose 2011) which is an extension to the MOD rule. Similar to WIP balance rules, some due date control rules can perform as global rules to improve pace of lot movement and increase on-time delivery. By noticing the supreme performance of lateness variance reduction, some rules can aim at optimizing a local manufacturing stage in terms of cycle time variance minimization (Zhou and Rose 2013).

Although the WIP balance rules lead to a significant reduction of WIP variability and the due date control rules bring well-paced lot movement toward on-time completion, we realized that WIP balance rules do not always lead to good due date performance and due date control rules do not primarily bring low WIP levels. Both WIP balance rules and due date control rules turn out to be insufficient when both targets, i.e., lower WIP level with lower cycle time, better on-time delivery and less tardiness, are desired simultaneously. This motivates us to develop some sophisticated and effective global rules combing WIP balance and due date control, e.g., matrix table (Zhou and Rose 2012b), Infineon global rule (Zhou and Rose 2012a) and WIP control table combining with ODD (Zhou and Rose 2013).

2.2 Target WIP Estimation

The second component, 'target WIP estimation', is responsible for providing target WIP for the other three components. Target WIP plays an important role in this framework due to the facts that: (1) In the first component, some WIP balance rules like MIVS, LB, MWVS and WIPCT utilize target WIP to determine if an operation or a work-center is high-loaded or low-loaded; (2) In the third component, real-time shop floor control applies target WIP to monitor the status of some specified work-centers or the whole fabs; (3) In the fourth component, target WIP can be employed to correct WIP imbalance. This component provides three methods, which are FIFO-based-simulation (Zhou 2014), queuing model (Lin and Lee 2001) and neural network (Chambers and Mount-Campbell 2002), to estimate target WIP to each operation/work-center and the whole fabs. As many wafer fabs run with uncertainty of products volume mix and change almost daily lot release rate, this component produces not only static target WIP, but also dynamic target WIP according to the dynamic status of the fabs.

2.3 WIP Imbalance Monitor and Detection

Although the 'global and local rules' component provides a wide variety of sophisticated rules to control the material flow, as a matter of fact, none of these rules is intelligent enough to handle the production variations in wafer fabs. Consequently, WIP imbalance, i.e., some operations/work-centers have too much WIP while others have little WIP, occurs unavoidably. To set up correction actions to deal with WIP imbalance, the first step is to identify WIP imbalance when it occurs. The third component 'WIP imbalance monitor and detection' is with this purpose. It real-time monitors the status of individual operation/work-center and whole fabs. In case predefined events are triggered, it will inform the fourth component for correcting action.

Table 2 lists two methods to identify WIP imbalance in this component. The first method, predefining target WIP to individual operation/work-center and whole fabs, is straightforward and understandable. Higher than the target WIP is considered as WIP imbalance. The advantage of this method is we know exactly the location where WIP imbalance takes place. While the second method checks the throughput of specified manufacturing stages or the whole fabs regularly, for the reason that it assumes WIP imbalance interrupts the material flow and has impact on throughput. This method totally abandons target WIP, but it costs more effort to correct WIP imbalance because it does not know where the WIP imbalance is located.

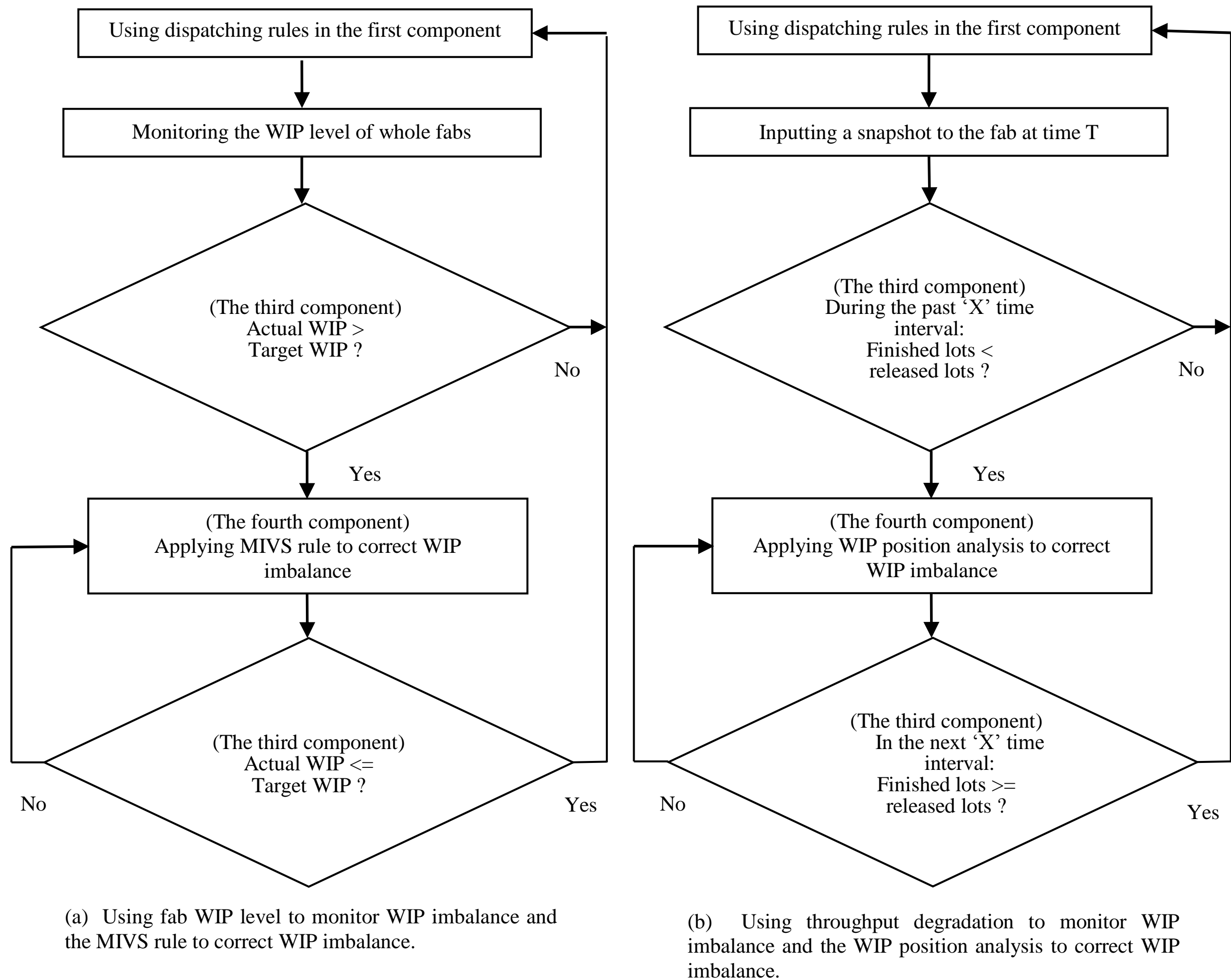
Table 2: Two WIP imbalance monitor and detection methods.

Method	Monitor	Detection
Target WIP	Monitor the actual WIP level of individual operation/work-center or the whole fabs continuously	If actual WIP > target WIP
Throughput degradation	Input a snapshot to the fabs	During the past 'X' time intervals, if throughput < release

2.4 WIP Imbalance Calibration

Finally, the 'WIP imbalance calibration' component takes action to correct WIP imbalance and smooth material flow after a WIP imbalance alarm is triggered by the third component. Corresponding to the two WIP imbalance detection methods above, this component provides two calibration procedures which are: (1) Using target WIP for detection and MIVS rule for correction; (2) Using throughput degradation for detection and WIP position analysis for correction, as illustrated in Figure 2.

To correct WIP imbalance, the most common way is to regulate the workload of each operation/work-center to prevent a small imbalance problem from being enlarged. The MIVS rule, which intends to keep the actual WIP close to target WIP, has proved to be effective in eliminating WIP imbalance. This is exactly what Figure 2 (a) tries to explain to us. After informed by the third component, it takes over the control of the first component and starts to correct WIP imbalances. It will release the control back to the first component if the actual WIP is lower than the target WIP, otherwise, it will continue the correction process. In reality, sometimes it is necessary to correct WIP imbalance for individual work-center interested instead of the whole fabs. This correction procedure can be extended in a flexible way, i.e., only monitoring the actual WIP of specified work-center and applying the MIVS rule in its upstream work-centers.



(a) Using fab WIP level to monitor WIP imbalance and the MIVS rule to correct WIP imbalance.

(b) Using throughput degradation to monitor WIP imbalance and the WIP position analysis to correct WIP imbalance.

Figure 2: Two different WIP imbalance calibration procedures.

Figure 2 (b) presents a different way to correct WIP imbalance by observing that throughput decrease is a symptom of WIP imbalance. If throughput has a sudden degradation, WIP imbalance definitely occurs 'somewhere', which causes WIP accumulation in the fabs. In this case, we have less concern about the accurate location of WIP imbalance, as target WIP is not involved. On the contrary, the challenge is how to make sure the throughput goes back to the right level. Simply speaking, to correct WIP imbalance we have to increase the throughput. Thus, WIP position analysis is applied to smooth material flow and

speed up lot movement. WIP position analysis is a WIP control and tracking mechanism that considers material flow from the viewpoint of operation (Zhou and Rose 2012b). It divides the material flow into some intermediate control units called 'Blocks', and one 'Block' consists of some consecutive operations. On one hand, by calculating the sum of the WIP of each 'Block' we are aware which congested 'Block' should push WIP to downstream to ensure throughput. On the other hand, by analyzing WIP evolution inside each 'Block', we are able to push WIP from congested operations to starved operations.

3 SIMULATION EXPERIMENT AND PERFORMANCE ANALYSIS

This framework is successfully implemented and integrated into Factory eXplorer (FX) which is a commercial simulation package for factory models.

We test this framework with a small wafer fabs dataset MIMAC6 from Measurement and Improvement of MAnufacturing Capacities (MIMAC). We refer the interested reader to Fowler and Robinson (1995) for details. MIMAC6 is a typical complex wafer fabs model including:

- 9 products, 9 process flows, maximum 355 process steps.
- 24 wafers in a lot. 2777 lots are released per year under fab loading of 100%.
- 104 tool groups (work-centers), 228 tools (machines), 46 single processing tool groups, 58 batching processing tool groups.
- Sequence dependent setup, rework, MTTR (mean time to repair), and MTBF (mean time between failures) of tool group.

3.1 Applying Different Rules in the First Component to Control the Wafer Fabs

First of all WIP Control Table (WIPCT) and ODD rules are selected as global rules for WIP balance and due date control, respectively. We will shortly describe the WIPCT and ODD rules, and refer the interested reader to Zhou and Rose (2013). In the WIPCT rule, each upstream work-center maintains a WIP control table which contains current WIP information of all its downstream work-centers, e.g., target WIP level, actual WIP level, WIP difference and utilization. The objectives of WIPCT rule are: (1) Evaluating the pull requests of downstream work-centers; (2) Minimizing the deviation of actual WIP to target WIP of downstream work-centers. The ODD rule breaks up the slack time into as many segments as the number of operations of a lot. It strictly keeps lots at the right pace to meet the operation due dates through the fabs. ODD of lot i at operation p (ODD(i,p)) is defined as follows:

$$\mathrm{ODD}(i, p) = R_i + \mathrm{RPT}(p) \times \mathrm{DDFF} \tag{1}$$

where R_i is the release time of a lot, RPT(p) denotes the raw processing time for a sequence of operations from operation 1 to operation p (including operation p). DDFF is due date flow factor which is defined as the target cycle times divided by the raw processing time.

Secondly, as we indicated before, we can apply those rules in a flexible way since they can perform either as global rules to achieve global targets or as local rules for local optimization. Based on the Push-Pull Point concept (Perdaen et.al. 2012), we can couple push and pull dispatching rules to control the manufacturing line. Our idea is to find out the Push-Pull Point in the MIMAC6 fabs, and couple together WIPCT as the pull policy and ODD as the push policy.

In MIMAC6 fabs, we realized that work-centers in the furnace area are critical in terms of WIP control because: (1) WIP increases in front of them as they are at the beginning of the line; (2) They are the main cycle time contributors. In this case, the furnace area is considered as the Push-Pull Point in the MIMAC6 fabs. Thus, we intend to apply WIPCT as the pull policy to minimize the mismatch between incoming and outgoing WIP for the work-centers of furnace area (there are 24 work-centers), and ODD as

the push policy to steer material flow for the work-centers in other areas like photo, etch, implantation and probe (there are 80 work-centers). We denote this method as ODD&&WIPCT (in Table 3).

We consider average WIP, average cycle time, cycle time variance, percent tardy lots, and average tardiness of tardy lots as performance measures for the whole fabs. We run the simulation for 18 months with 3 replications, the first 6 months are considered as a warm-up period, and not taken into account for statistics. The fabs loading is 95% which is considered as high loading. In Table 4 12 months of simulation results are illustrated.

Table 3: Three different rules to control MIMAC6 fabs.

Dispatching rule		Target	
		Global rule	Local rule
WIPCT (pure pull)		WIP balance	
ODD (pure push)		Due date control	
ODD&&WIPCT (push&&pull)	ODD (push)	Due date control for 80 work-centers of manufacturing areas like photo, etch, implantation and probe	
	WIPCT (pull)		Local WIP optimization for 24 work-centers of furnace area

From the simulation results, in principle we cannot draw a safe conclusion that whether WIPCT (WIP balance) outperforms ODD (due date control), and vice versa. As WIPCT produces better results than ODD with regard to average WIP and cycle time, and ODD shows supreme performance over WIPCT with respect to cycle time variance, on-time delivery and tardiness. Whereas, the outstanding performance deriving from ODD&&WIPCT gives us a way to achieve both WIP balance and due date control concurrently. In fact, the biggest advantage of this framework is a wide variety of WIP balance and due date control rules are integrated into it. Dispatching rules are still the most common tools for shop floor control and only applying a single rule has proved to be less effective in achieving multiple performance objectives (Dabbas and Fowler 2003). The successful examples, such as matrix table (Zhou and Rose 2012b), Infineon global rule (Zhou and Rose 2012a) and ODD&&WIPCT, indicate that there is potential room to improve the efficiency and productivity of shop floor control if we can take advantage of these rules to serve our purposes by means of different applications as described in Table 1.

Table 4: Five performance measures of MIMAC6 fabs under the control of four rules.

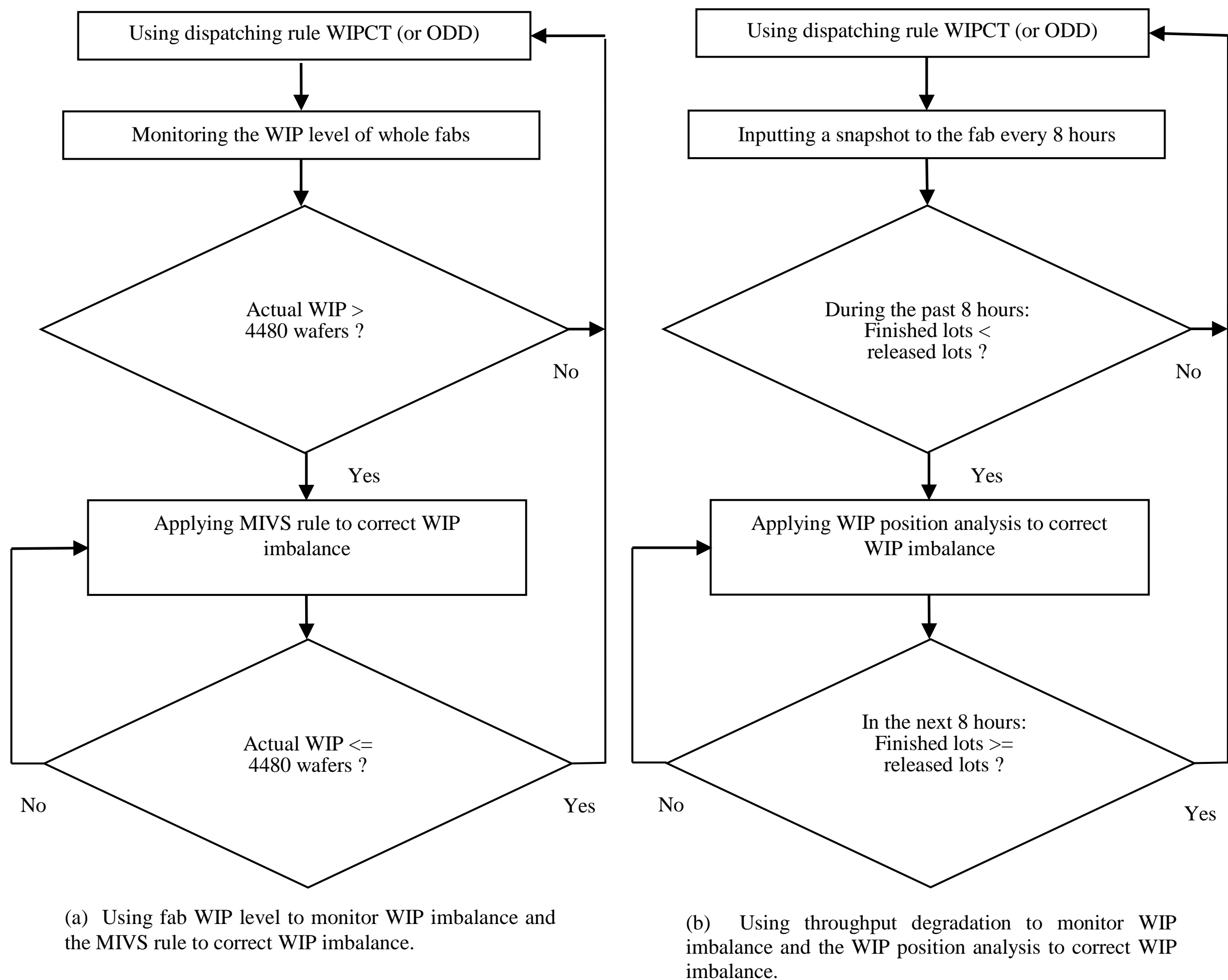
	Avg. WIP (wafers)	Avg. cycle time (days)	Cycle time variance (days^2)	Percent tardy lots (%)	Avg. tardiness of tardy lots (days)
FIFO (2.2 DDFF)	4943	29.6	1.65	28.8	1.0
WIPCT (2.2 DDFF)	4696	27.8	4.60	9.8	0.8
ODD (2.2 DDFF)	4765	28.5	0.35	0.4	0.05
ODD&&WIPCT (2.2 DDFF)	4454	26.2	0.50	0	0

Where DDFF stands for due date flow factor.
Due date is calculated as: Release time + Raw processing time * DDFF

3.2 WIP Imbalance Correction for WIPCT and ODD Rules

This section will explain two test cases which apply the WIP imbalance calibration procedures described in Figure 2 to correct the WIP evolution curves of the WIPCT and ODD rules.

Before the simulation experiment, we explain the following fact. The target WIP applied in WIPCT rule is derived from queuing model in the second component. In WIPCT, each work-center has a target WIP, and the sum of the target WIPs of all work-centers is 4480 wafers that are considered as the target WIP of whole fabs. In fact, the actual WIP of whole fabs derived from the WIPCT is 4696 wafers (Table 4). This is higher than the target WIP. It turns out that the WIPCT still cannot accomplish its task in spite of its effort to keep the actual WIP close to the target WIP. Relatively speaking, the WIPCT cannot handle WIP imbalance perfectly, which results in a higher deviation to target WIP. Therefore, we are interested in finding out whether the difference between actual WIP and target WIP can be minimized when the WIP imbalance calibration is applied.



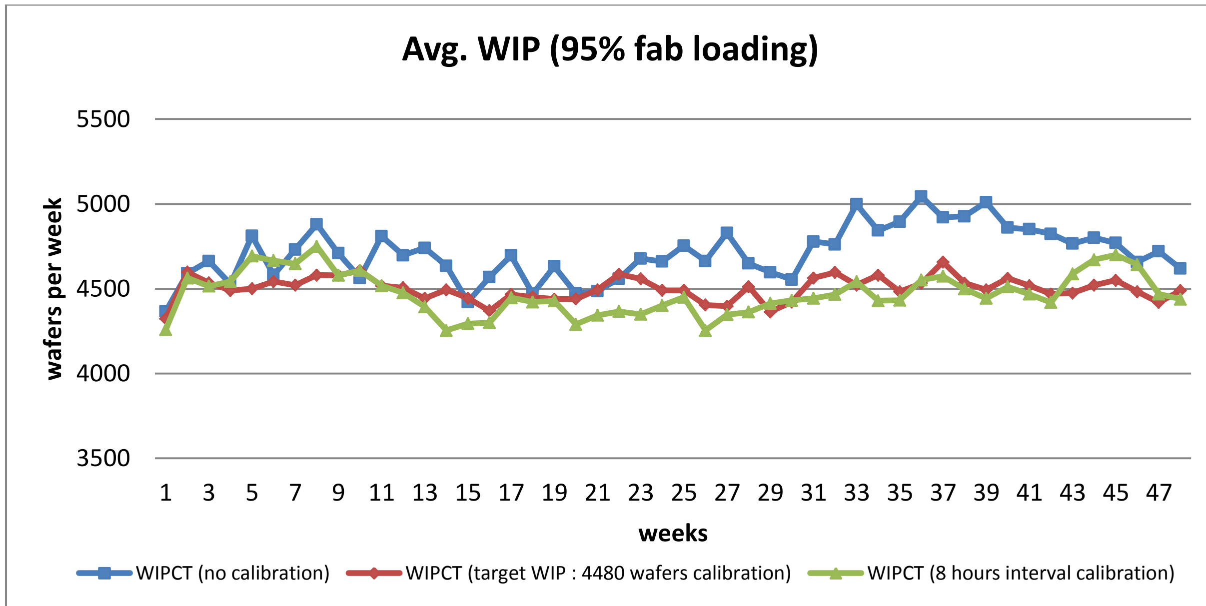
(a) Using fab WIP level to monitor WIP imbalance and the MIVS rule to correct WIP imbalance.

(b) Using throughput degradation to monitor WIP imbalance and the WIP position analysis to correct WIP imbalance.

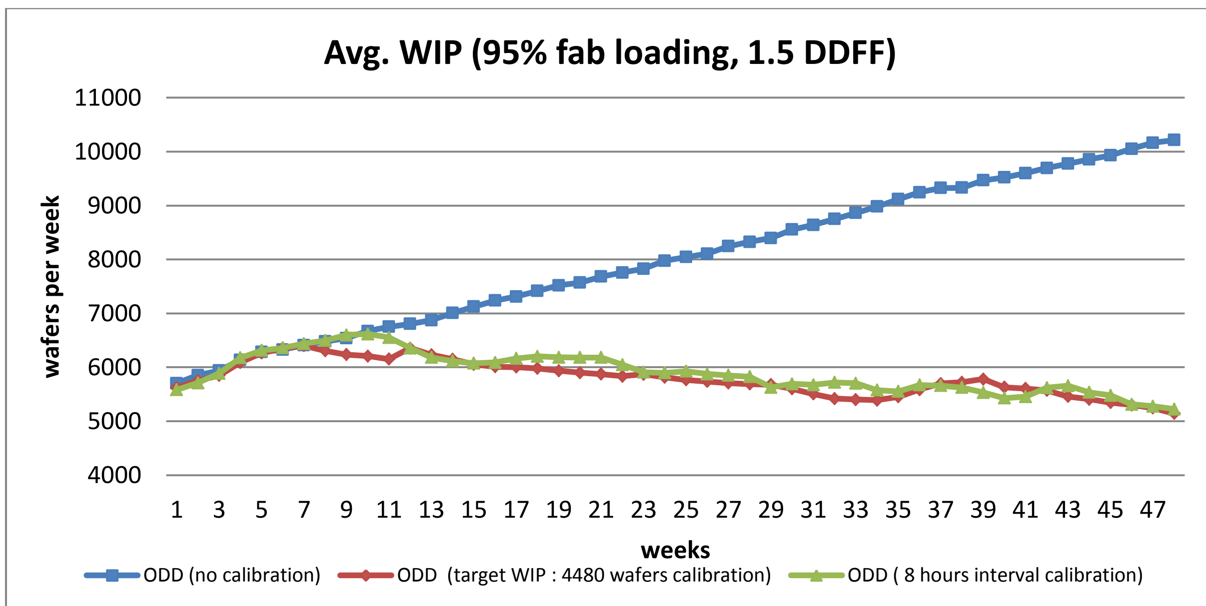
Figure 3: Two test cases to correct WIP imbalance for WIPCT and ODD rules.

We notice that it is not a trivial task to employ due date control rules since they rely on proper target due dates. Serious WIP congestion might arise if the fabs run products with tight target due dates and under high loading, which is considered as WIP imbalance phenomenon reported by Zhou and Rose

(2011). For the second test case, we apply the ODD rule in MIMAC6 fabs with a tight target due date flow factor 1.5 and under 95% fab loading. We expect the increasing WIP evolution curve caused by ODD is prevented by WIP imbalance calibration as well. The simulation experiment settings of these two cases are described in Figure 3. The WIP evolution curves of 48 weeks of WIPCT and ODD with/without calibration are demonstrated in Figure 4.



(a) WIPCT



(b) ODD

Figure 4: WIP evolution curves of WIPCT and ODD with/without calibration.

From Figure 4 (a), we can get a clear picture that both calibration procedures are able to lower and smooth the WIP curve of WIPCT. The difference is the calibration applying 4480 wafers as target WIP

can exactly maintain the actual WIP around the target WIP, and the other applying without target WIP deviates from 4480 wafers relatively higher. Likewise, from Figure 4 (b) it is obvious that both calibration procedures successfully prevent the WIP curve from increasing. These two procedures behave slightly different. The one applying target WIP responds faster as it stops the WIP accumulating starting from the 8th week, while the other applying without target WIP starts from the 11th week.

In this study, we have no intention to judge the merits of these two calibration procedures, since they both have the pros and cons. As a matter of fact, the WIP imbalance calibration we proposed illustrates about how to enhance the intelligence of automated manufacturing. In real wafer fabs, production managers spend considerable effort to cope with WIP imbalance to ensure material flow in an affluent fashion. The joint effort of components ‘WIP imbalance monitor and detection’ and ‘WIP imbalance calibration’, actually, brings a feasible way to assist production managers to track WIP imbalance, develop corresponding strategy and initiate automated lot dispatching.

4 CONCLUSION AND OUTLOOK

In this paper, we presented a framework to deal with shop floor control problems, which are: (1) How to solve the conflicting goals between WIP balance and due date control; (2) How to reduce the impact of WIP imbalance which cannot be handled by WIP balance rules or due date control rules, in wafer fabs. We introduced this framework via elaborating the major functionalities of each component and demonstrating the interactions between each component. We carried out two simulation experiments to point out that this framework provides substantial toolsets to solve those two shop floor control problems. Particularly, we highlighted the following two facts: (1) Regarding the basic control strategies in wafer fabs, the first component comprising different kinds of dispatching concepts enriches the way to control material flow to improve specific performance indicators; (2) The benefit gained from the joint effort of the third and fourth components that the material flow (WIP evolution curve) is significantly improved. It demonstrated a possible way to enhance the real-time automated manufacturing intelligence, as it brings effective real-time WIP imbalance notification triggered by events such as exceeding target WIP threshold or throughput degradation, and enables automated WIP imbalance correction via analyzing and tracking dynamic WIP position.

In order to make this framework more applicable for shop floor control, the following two aspects should be implemented: (1) As batch and setup are two causes for WIP variability, incorporating different batch and setup rules as local optimization strategies is one way to reduce variability effect. Furthermore, it is interesting in finding out whether the local batch and setup optimizations have positive or negative effects on overall fabs performance; (2) The ways to monitor WIP imbalance can be more flexible by introducing a due date violation threshold. By noticing misleading target due date may cause WIP imbalance, using due date violation threshold, such the percentage of lots that are out of schedule or what is tardiness, provides a global view of due date performance to monitor the status of fabs.

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