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IMPROVING CLUSTER TOOLS PERFORMANCE USING COLORED PETRI NETS IN SEMICONDUCTOR MANIFACTURING

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ABSTRACT

Semiconductor manufacturing is a capital-extensive industry. How to utilize billions of dollars of equipment as efficiently as possible is a critical factor for a semiconductor manufacturer to succeed in stiff competition. Improving performance of manufacturing process increases overall tool throughput, reduces operating costs, and saves companies millions of dollars. In this study, we develop a methodology to analyze and improve a cluster tool's performance. A Colored Petri Net model is developed to determine internal bottleneck resource of the tool. Results conclude that the methodology improves tool efficiency and provides significant cost savings.

1 INTRODUCTION

Semiconductor manufacturers are required to reduce their product cycle times since many products embedding semiconductor devices often have a very short life cycle. One way to reduce cycle time is to purchase extra manufacturing tools. However, these tools cost several millions of dollars and facility space is very limited. Another way to reduce cycle time is to improve performance of the critical tools. The second option is less costly and provides a significant cost saving for manufacturers, which leads them to maximize efficiency.

Memory chips are produced by a multi-step processing of silicon discs, called "wafers". A part type undergoes about one thousand complex processing steps, including photolithography, etching, chemical and physical vapor deposition, cleaning, and thermal processing. Among these processes, dry etching is one of the critical processes since it constitutes about 12% of total production time. Thus, improving capacity of the dry etching process yields lower product cycle time, which motivates this study.

Cluster tools are highly integrated machines that can perform a sequence of manufacturing processes. A series of processing steps, transportation, and control are integrated into a single tool (Singer 1995). We study the cluster tools for dry etching process (called Dry Etch tools) in semiconductor manufacturing that consist of different resources including three load ports (LP1, LP2, LP3), one wafer transfer robot in atmosphere (ATM) with a single arm, one aligner (AG), two airlocks (AL1, AL2), one wafer transfer robot in vacuum (VTM) with double arms, and four process modules (PM1-PM4) (see Figure 1).
AG and ATM are in atmospheric pressure (called atmosphere). The resources VTM, and PM1-PM4 are in vacuum pressure (called vacuum), which is less than atmosphere. A load port is the interface of the cluster tool to the manufacturing floor. The delivery system places a lot, which is processed in the cluster tool, onto the load port. The load port is isolated from the outside environment by closing the external door.

A robot is the transport mechanism that is responsible for moving the wafers within the cluster tool to the individual process stations. The tool has two robots: ATM and VTM. ATM is a robot arm, which can

move along Y and Z axes (Brooks Automation 2012). VTM robot has two dual-blade type handles, which can move along X,Y, and Z axes (Brooks Automation 2012).

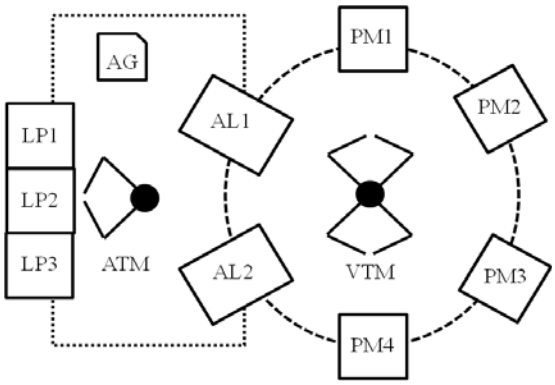

Figure 1: Dry Etch cluster tool

Airlocks are the gateways between atmosphere and vacuum (Paek and Lee, 2002). An airlock has two doors; one in atmosphere and one in vacuum. The time required to adapt the airlock environment to the conditions within the vacuum section of the mainframe is called pump time. The time it takes to adjust airlock to the atmosphere conditions of the cluster tool is called vent time. Each airlock in the tool has two wafer slots dedicated for unprocessed and processed wafers, respectively.

Process modules (PMs) (chambers) are responsible for performing the material processing. Only a single wafer is processed in a process module. Depending on the type of process performed in the module, a chamber is also responsible for generating the environmental conditions. PM runs four types of processes including chamber heating/cooling, etching, chamber cleaning, and pressure control. Durations of these processes are based on a recipe attached to a lot. Chamber heating/cooling process adjusts chamber temperature based on limits provided in the recipe. PM runs this process once before a wafer is processed. Etching process removes masked pattern from the wafer. Cleaning process starts after the wafer leaves chamber. Pressure control checks the pressure in the chamber when all wafers are processed.

The scheduler is the component of the cluster tool, which determines sequence of wafers processed on each tool resource. Particularly, a schedule includes information of process start and end times for ATM, AL, VTM, and PM activities (called states). Each resource has an active state where it is occupied by a wafer and an idle state where it is waiting for a wafer to arrive or for a wafer to be picked up. Each active state of a resource corresponds to a job.

The sequence of instructions generated by the scheduler defines a scheduling plan of the cluster tool resources, which can be visualized using a Gantt chart. States for tool resources are marked using different colors. Figure 2 illustrates a Gantt chart example for a wafer in a lot in the dry etch cluster tool. In the schedule, ATM picks a wafer from a lot and places it on aligner where wafer is aligned. ATM waits with wafer on aligner until process is completed. Then, AL1 door in atmosphere opens and ATM drops wafer. After wafer is delivered, AL1 atmosphere door closes and AL1 pumps to vacuum with wafer. After pumping is completed, AL1 vacuum door opens, VTM picks wafer, PM1 door opens, and VTM drops wafer in PM1. PM1 accepts wafer after it runs heating/cooling processes to reach a certain temperature level. After VTM drops wafer, PM1 door closes and etching process starts. After etching process ends, PM1 door opens and VTM picks the processed wafer. PM1 door closes and chamber cleaning process starts. AL1 vacuum door opens and VTM inserts the processed wafer. AL1 door closes and vents to atmosphere. Once venting is finished, AL1 atmosphere door opens and ATM picks wafer and delivers it to a load port. Observe that PM1 performs pressure check after each lot is completed.

The Dry Etch cluster tool runs in a parallel configuration where all process chambers perform an identical process step (Koehler et al. 1999). The tool operates in a single mode where the tool processes the wafers of only one lot at a time. When all wafers are processed, the lot is removed from the load port,

a new lot is loaded and the cluster tool starts processing wafers from the new lot. The cycle time of a lot is the time when the lot is placed into one a load port until it is removed from the load port with all wafers in the lot being processed.

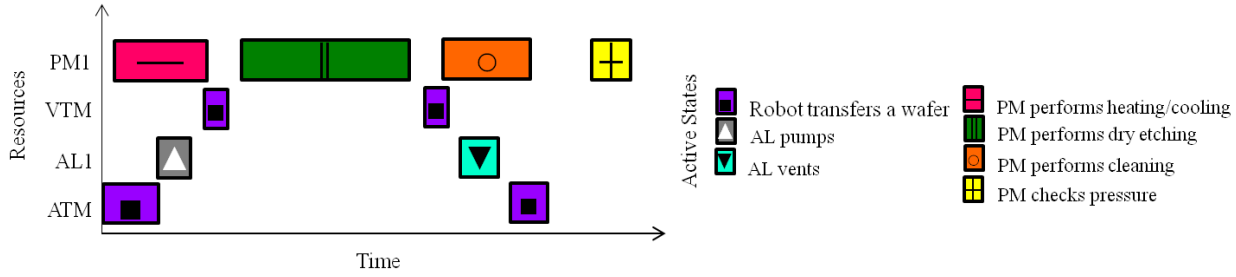

Figure 2: An example of wafer movement in the tool

The objective of this study is to improve performance of the dry etch cluster tool, which is described above. Dry etch cluster tool scheduling problem (DE-CTSP) is to determine a schedule for the dry etch cluster tool with minimum lot cycle time. A cluster tool with load ports, a transfer robot and process chambers, can be modeled as a robotic flow shop where load ports and chambers are equivalent to input stations and machines, respectively. The cluster tool sub-problem is to schedule a given number of wafers (jobs) on chambers (machines) to minimize cycle time. Crama and van de Klundert (1997) show that the robotic flow shop problem, which is equivalent to the cluster tool sub-problem, is strongly NP-Complete (Garey and Johnson 1979). Since the cluster tool problem is a subset of DE-CTSP, the general version of DE-CTSP is NP-hard. Therefore, there is no algorithm which provides an optimal solution for the problem in polynomial time unless P=NP. Note that there may exist polynomial time algorithms for specials cases of the problem.

Since DE-CTSP is NP-hard, we develop a simulation model of the cluster tools based on Colored Petri Nets (CPNs), which enables us to run various what-if scenarios. Using the simulation model, we evaluate and improve performance of the dry etch cluster tools in a semiconductor manufacturer. We employed the CPN formalism for the advantages it offers due to its graphical modeling language and a well-studied suite of analytical tools supporting it. Note that the results presented in this paper were obtained by running simulations on the CPN model. A number of future studies will involve the use of state space analysis of the CPN model to address performance, utilization, and scheduling related issues of interest.

This paper is organized as follows. Section 2 provides an overview of approaches for modeling cluster tools. Section 3 provides the detailed description of the simulation model that we develop. In Section 4, we present our tool analysis consisting of different case studies. Section 5 provides a summary of this research and discusses future research directions.

2 LITERATURE

Subsets of DE-CTSP can be reduced to problems such as robotic flow shop scheduling problem, parallel machine scheduling problem and parallel machine scheduling problem with transporters. There exists a large body of literature on these problems, but there are only a few known studies, which consider the exact DE-CTSP in the literature.

Lee (2008) provides a detailed review of cluster tool architectures, operational issues and scheduling requirements, and explains recent progress in tool science and engineering for scheduling and control of cluster tools. The dry etch cluster tool we study is classified as a cluster tool with intermediate buffer in the literature.

There exist studies in the literature, which consider different configurations of the dry etch cluster tool to analyze and improve its performance. The approaches presented in the literature involve the use of discrete event simulations for performance analyses, use of heuristics for the solution of scheduling problems and closed-form formulations for the behavior a tool and/or tool part (Pederson and Trout 2002, Un-

behaun and Rose 2007, Christopher 2008). However, analysis and improvement of the dry etch cluster tool using these reported approaches is not general enough because of the level of abstraction used, or by the simplifying of assumptions made in each of them. In our study, ATM, airlock, VTM and chamber resources interact with each other, as well as perform individual tasks. An analysis model detailed enough to capture the complexity of semiconductor manufacturing tools and their internal components is required to study the effects of different production recipes, control and architecture, wafer waiting times and sequencing.

Petri Nets (PNs) are a graphical and mathematical modeling formalism for design and analysis of Discrete Event Systems (DESs). The theory of PNs has been evolving as a powerful tool for the modeling, design, analysis, planning, scheduling, control and implementation of manufacturing systems. The characterization of a manufacturing system as a Discrete Event System (DES), exhibiting features as concurrency, asynchrony, non-determinism, mutual exclusion, resource sharing, deadlocks, routing flexibility and lot sizes, allows the use of PNs for modeling and analyzing its dynamical behavior. In the last two decades, PN modeling has gained more and more attention in the semiconductor manufacturing applications due to its graphical and mathematical advantages over traditional tools to deal with discrete-event dynamics and characteristics of complex systems. Jeng and Zhau (1998) provide an overview of some of the earlier applications of PN theory to the semiconductor manufacturing systems. Srinivasan (1998) and Shin and Lee (1999) are some of the early works that models cluster tools using timed PNs. Zuberek (2000) considers a simple cluster tool with multiple chambers, a single robot and one load lock, and develop a PN model to derive the steady–state, as well as the initial and final transient behavior of the tool. Jung and Lee (2008) use PN modeling to develop a mixed integer programming model to maximize the throughput rate of a semiconductor manufacturing system. Lee and Lee (2010) develop PN models for modeling and specifying the tool architecture, the wafer flow pattern or the recipe, the scheduling requirements, the tool behavior, and the scheduling rules. Hsu et al (2010) uses the PN modeling for the optimization of tool operation sequence for efficiency. They use the PN model to mathematically formulate the optimization problem.

CPN is an extension of the ordinary PN theory. A number of other extensions to PN theory can be found in the literature, however, the CPN theory is general enough to encompass most, if not all, of the features present in the others. All these extensions to the basic theory of PNs are called High Level nets. The concept of Hierarchical PNs is also incorporated in CPN theory to develop modeling tools with support for modularity and abstraction. More advanced material on CPN can be found in Jensen and Kristensen (2009). Su and Wang (2010), and Cao et al. (2010) apply the hierarchical Colored-Timed Petri nets for scheduling semiconductor manufacturing systems.

3 APPROACH

We now present our methodology to analyze and improve the dry etch cluster tool based on CPN. A hierarchical CPN model of the tool, described in Section 1, is developed using CPN Tools software application (CPN Tools 2012). The top-page view of the model is shown in Figure 3. The transitions in this model correspond to the components LP1, LP2, LP3, ATM, AL1, AL2, VTM, and PM_i ($i = 1,..., 4$) of the cluster tool described in Section 1. Each rectangular node in this model is a substitution transition, which means that it contains a more detailed component model on a sub-page. A model of each of these components is developed at a level of detail that is amenable for the required analysis. The following is a brief description of each of the components in the model.

3.1 ATM and VTM Robots

The single-armed ATM robot at the atmospheric side of the tool is modeled as a resource place in the CPN model (Figure 3). As part of its functionality described in the previous section, the place labeled ATM carries a single token that signals both availability and status of the robot. The color (or value) of a token in ATM place is defined as an ordered tuple:

((<wafer_status>, <wafer_id>), <location>)

where *<wafer_status> ∈ {none, unprocessed, processed}*

<wafer_id> ∈ {-1} ∪ Z+

<location> ∈ {Home, LP1, LP2, LP3, Al, AL1, AL2}

A special token *((none, -1), Home)* is used to indicate the condition when ATM is idle and available to perform an assigned activity.

The VTM robot at the vacuum side has two arms to hold processed and unprocessed wafers. The two arms are connected to the same actuator, which allows one arm perform a task while the other sits idle (see Section 1 for more details). In the CPN model of Figure 3, VTM is modeled as a resource place. This place carries a single token with the following token structure:

((<wafer_status>, <wafer_id>), (<wafer_status>, <wafer_id>))

where *<wafer_status> ∈ {none, unprocessed, processed} and <wafer_id> ∈ {-1} ∪ Z+*

In this definition, the two ordered pairs correspond to the status of the two arms of VTM. The special token value of *(none, -1)* is used to depict an empty (and available) VTM arm.

The specific functions performed by both ATM and VTM at each component of the tool are discussed further in the descriptions of other components in the tool.

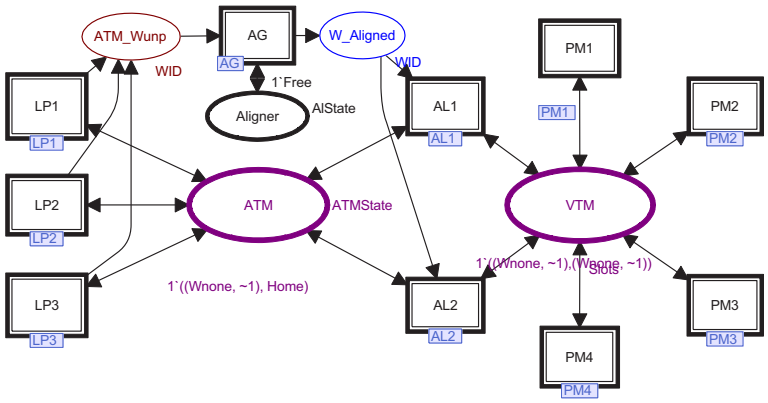

Figure 3: Top-page view of the CPN model

3.2 Load Ports (LP)

The three load ports on the tool have similar Petri net structures in the model. These structures may differ from each other due to different values assigned to parameters that represent time delays assigned to activities modeled as transitions. Figure 4 shows the detailed model of LP1 that is implemented on a subpage in CPN Tools.

The input place labeled LP1 (in Figure 4) models the wafer lot as a pair of two integer lists. The integers are used to assign wafer ids. The first lists the unprocessed wafers and the second lists the processed wafers in a lot at the load port. More formally, the color (or value) of a token in LP1 place is defined as an ordered pair:

(<list_of_unprocessed_wafers>, <list_of_processed_wafers>)

where *<list_of_unprocessed_wafers> = [1, 2, 3, ..., n], n ∈ Z+*

<list_of_processed_wafers> = [1, 2, 3, ..., m], m ∈ Z+

The two lists can also be null (i.e., []) for conditions where there are no unprocessed wafers left in the lot and when a new lot with only unprocessed wafers is loaded on a load port. The transitions in Figure 3, i.e., *PutWLP1* and *PickWLP1*, depict the activities that ATM performs at the load port. These transitions are assigned delay parameters that are user-defined.

3.3 Aligner (AG)

Once an unprocessed wafer is picked up by ATM, it is aligned at AG before it is put in an airlock for transportation to the vacuum side of the tool. Figure 3 shows the aligner as a transition-place pair labeled as AG. A user-defined delay parameter is assigned to the transition that models the alignment process. The place labeled Aligner keeps track of the state of AG. A token in this place can have one of two possible values:

<aligner_status> ∈ {Busy, Free}

3.4 Airlocks (AL1, AL2)

The CPN model of the cluster tool contains two airlocks for transporting wafers between atmospheric and vacuum sides of the tool. In this model, each airlock is equipped with a pair of slots for holding wafers. Both airlocks have similar Petri net structures in the model. The CPN model of an airlock also provides a provision for a user to run it with a number of different behavioral schemes. For example, one scheme reserves a slot in each airlock for processed wafers and another for unprocessed wafers.

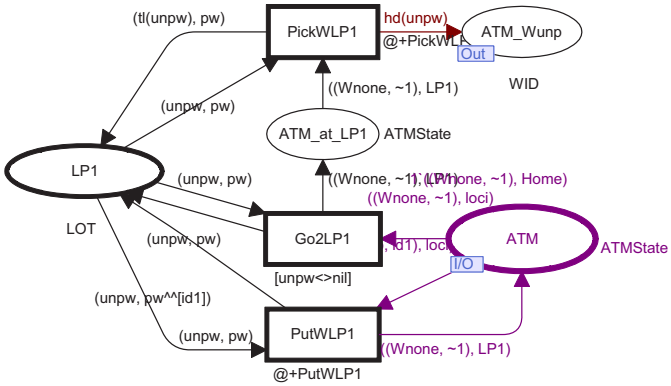

Figure 4: Detailed CPN model of a load port

In the CPN model of an airlock model, an unprocessed wafer can be seen traveling from left to right (as a sequence of transitions) and a processed wafer from right to left. These transitions can be divided into three sets: (1) transitions on the left-hand side represent interactions between airlock and ATM at the atmospheric side, (2) transitions on the right-hand side represent interactions between airlock and VTM at the vacuum side, and (3) transitions in the middle represent airlock activities, i.e., switching between atmospheric and vacuum. A pair of transitions is used to implement a switch from atmospheric side to vacuum and from vacuum to atmosphere. One of these two transitions, e.g., *Atm2Vac*, implements the switch from atmosphere to vacuum during steady-state (when processed wafers are being removed from vacuum side, modules are processing the wafers and new unprocessed wafers are being transported to vacuum side.) This transition requires that there must be at least one unprocessed wafer in one of the two slots before the switch. The second transition, *Atm2Vac_Empty*, implements the special switch during the final phase when the last four processed wafers are being removed from the PMs. During this phase, airlock makes empty switches from atmosphere to vacuum to bring back the last few wafers from the vacuum side. Similarly, the transition *Vac2Atm_Empty*, implements the empty switches from vacuum to atmosphere during the initial phase when new unprocessed wafers are being loaded into the system for the first time.

The color (or value) of a token in AL1 place is defined as a tuple:

(<pressure_status>, ((<slot1_status>, <wafer_id>), (<slot2_status>, <wafer_id>)))

where *<pressure_status> ∈ {atmosphere, vacuum}*

<sloti_status> ∈ {none, processed_wafer, unprocessed_wafer}

$<wafer\_id> \in \{-1\} \cup Z^{+}$

3.5 Process Modules (PM1-PM4)

Once an unprocessed wafer is brought to the vacuum side by an airlock, the wafer is picked up by VTM on one of its two arms. The wafer is then taken to an available process module to be processed. A CPN model of one of the four PMs used in this study is shown in Figure 5. The other modules have similar CPN structures. In Figure 5, the transitions *PutWPM* and *TakeWPM* model the activities where VTM puts and removes a wafer from a module. All the other transitions in the model (Figure 5) correspond to the activities of a process module. The transitions labeled *WWH*, *WAC*, and *PAC* represent module heating/cooling and cleaning steps performed by the module at different points during processing a of lot.

In Figure 5, the place *PM1* in the middle keeps track of the state of the process module. The *color* (or value) of a token in *PM1* place is defined as an ordered pair:

(<pm_status>, <wafer_id>)

<pm_status> ∈ {clean, unprocessed_wafer, processed_wafer, unclean}

$<wafer\_id> \in \{-1\} \cup Z^{+}$

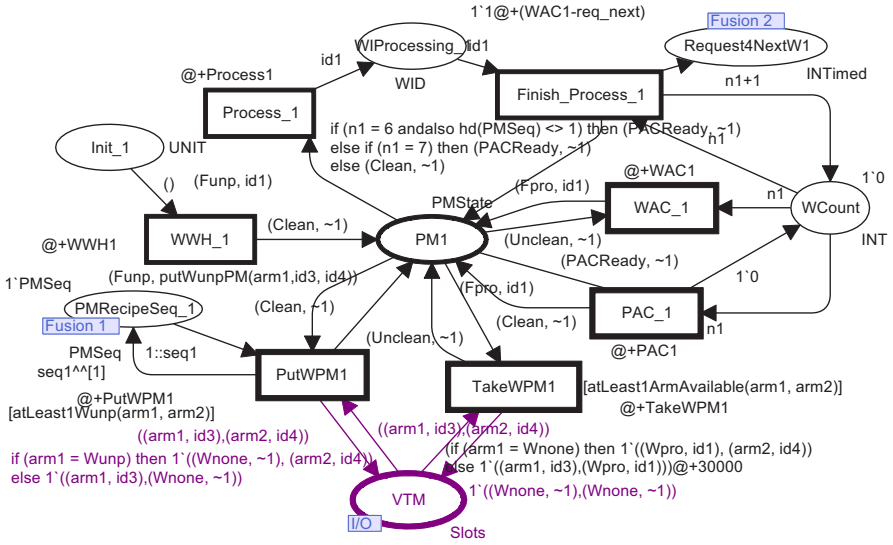

Figure 5: Detailed CPN Model of a process module

4 ANALYSIS

We analyze and improve performance of a dry etch cluster tool in a semiconductor manufacturer. Using tool scheduling data, we develop Gantt charts (Figure 6) to understand tool behavior. Table 1 illustrates parameters that are used in the CPN model.

Table 1: Data collected from DE-CST

Resource	Data
ATM	Transfer times from LP1-LP3 to AL1, AL2 and from AL1,AL2 to LP1-LP3
AG	Duration of aligning process
AL	Duration of pump and vent
VTM	Transfer times from AL1,AL2 to PM1-PM4 and from PM1-PM4 to AL1,AL2
PM	Durations of heating/cooling, etching, cleaning, and pressure check processes

The DE-CST tool has the following characteristics. Durations of pump and vent are equal for AL1 and AL2. PM1-PM4 has an equal heating/cooling and cleaning processes duration. Cleaning process time

is proportional to etching process time. Similarly, the duration of pressure check process is equal for PM1-PM4. The heating/cooling process runs before each lot for each process chamber, and cleaning process runs after each wafer processed in a chamber. The pressure check process runs after each lot is processed in a chamber. Wafers are assigned to chambers in order of PM1-PM4.

The objective of the analysis is to reduce lot cycle time of DE-CST using the CPN model. We first identify bottleneck resource in the tool and then improve performance of the bottleneck using the simulation model. Note that we may have different bottlenecks in the tool for different recipes. In the analysis, we use the CPN model to compare the base case scenario, which is the current tool schedule, with the alternative scenarios.

4.1 Base Case

Figures 6 illustrates a base case schedule for DE-CST for Recipe 0, which is the most frequent recipe run on the tool. In the schedule, one lot is processed with twenty five wafers. The slot numbers of wafers in the lot are illustrated in the etching processes as "W#". Observe that heating times for the production recipe is zero.

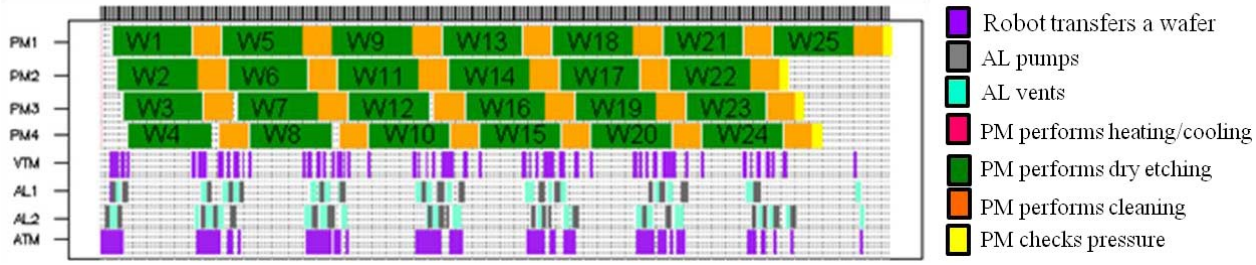

Figure 6: Base case for a production recipe

The size of the base case problem is large. If the problem is modeled as a mixed-integer program, then there are approximately 2500 binary and 275 continuous variables, and 2250 constraints.

4.2 Identifying and Improving the Bottleneck Resource

In a traditional manufacturing line, the workload of a process step is the sum of the process times of all jobs for the step.. Imbalance in the workloads of the process steps cause waiting of the jobs or work-in-progress. However, in cluster tools, the workload is not easy to define because the material handling system (robots, airlocks) interferes with the job processing cycle (Lee 2008). Bottleneck of a cluster tool is a tool resource which restricts the rate of wafer processing, leading to low throughput and higher cycle time (Srinivasan 1998). If the bottleneck resource is identified, then it is sufficient to improve throughput of this module to improve the overall tool throughput.

The CPN model is used to run different what-if scenarios to identify the tool bottleneck and characterize the recipes. In the scenarios, we increase the performance of each resource linearly one at a time, and measure the rate of cycle time decrease as a result of this improvement, comparing with the base case. Definitions of resource performance improvement are provided for each resource in Table 2. Let c_j be the lot cycle time for the scenario j (or recipe j) and c_0 be the lot cycle time value for the base case scenario. Lot cycle time reduction, CTR_j, for scenario j is calculated as using the following equation.

$$CTR_j = \frac{(c_0 - c_j)}{c_0}$$

Note that if CTR_j <0, the lot cycle time is increased in scenario j.

We now identify the bottleneck resource in the tool for Recipe 0.. We investigate five different scenarios using the CPN model in order to identify bottleneck (see Table 2). The "Etch Time Red." scenario reduces both etching times and cleaning times in PMs.

Note that pump and vent speed for both airlocks are increased in "AL Pump/Vent Inc." with same rate.

We observe that increasing ATM and VTM robots speed, and pump and vent times for airlocks do not provide significant throughput increase unless production recipes are improved, as is shown in Figure 7a. Note that if the robot speed is higher than a threshold, then the robot cannot hold a wafer without sliding. Similarly, if airlock pump/vent speed is higher, then particles form a cloud within airlock, and some of these particles may land on the wafer surface, which causes significant quality problems. In order to improve aligner speed, a new hardware design is required, which is costly for a small improvement. Thus, VTM, AL, aligner, and ATM performance improvements are limited compared to PMs.

Table 2: Scenarios to identify bottleneck in the base case

Scenario Name	**Related Resource**	**Resource Improvement**
PM Etch Time Red.	PM1,PM2,PM3,PM4	Reduce etch and clean run times
VTM Speed Inc.	VTM	Increase robot speed
AL Pump/Vent Inc.	AL1, AL2	Increase pump/vent speed
ATM Speed Inc.	ATM	Increase robot speed
AG Inc.	Aligner	Increase aligning speed

We now identify bottleneck resources of DE-CST for a shorter recipe (called Recipe 1). Recipe 1 is the second most frequent run production recipe, and it has shorter etching and cleaning times than Recipe 0. Pressure check time is the same for both recipes. This analysis helps us understand performance characteristics of the tool when shorter recipes are run. Let I be the set of resources in DE-CST where $I=\{1,..,8\}$ and i=1,…,8 for ATM, AL1, AL2, VTM, PM1-PM4, respectively. Let u_{ir} be the busy time of resource $i \in I$ for recipe r where $r=0$ for Recipe 0 and $r=1$ for Recipe 1. Note that c_0 is the lot cycle time for Recipe 0 and c_1 is the lot cycle time for Recipe 1. The current resource utilization, CU_{ir}, for resource $i \in I$ and recipe $r \in \{0,1\}$ is defined as in the following formulation.

$$CU_{ir} = \frac{u_{ir}}{c_r}$$

Resource utilization, RU_{ir}, for resource $i \in I$ and recipe $r \in \{1\}$ is defined as

$$RU_{ir} = \frac{CU_{ir}}{CU_{i0}}.$$

Figure 7b illustrates CU values for resources for both recipes and RU for Recipe 1. Note that $RU_{i0}=1$ for all resources $i \in I$ for Recipe 0. We observe that PM1 is the bottleneck for Recipe 1 where $CU_{51} = 93\%$. Note that busy times for VTM and ATM are equal for both recipes since $CU_{10} = RU_{11}$ and $CU_{40} = RU_{41}$. Also, busy times for AL1 and AL2 are very close for Recipes 0 and 1. This means that ATM, AL1, AL2, and VTM are occupied at their maximum levels and speed improvement is required to improve their performance. As a result, there exists up to 7% cycle time improvement opportunity for Recipe 1 by increasing speed of ATM robots and speed of pump/vent times for airlocks, since they have the highest CU values other than process chambers.

We now show how to improve the bottleneck performance for the base case. Since PMs utilizations are close to 100%, the only way to reduce cycle time is to redesign production recipes. Note that since etch times are proportional to cleaning times; if we reduce etching times, then we can also reduce the cleaning times. If reducing etching times is not an option, there is still an opportunity for an improvement by reducing the cleaning times. We investigate both cases using the CPN model.

In addition to the "Etch Time Red." Scenario in Table 2, we run another scenario ("Clean Time Red.") to identify recipe time reduction opportunities for Recipe 0 on DE-CST.. The "Clean Time Red." Scenario only reduces cleaning times while etching times are fixed for the base case. Since the process times for the chambers are defined based on production recipes and each chamber runs the same recipe, once we reduce process times, we reduce them for all chambers with the same rate.

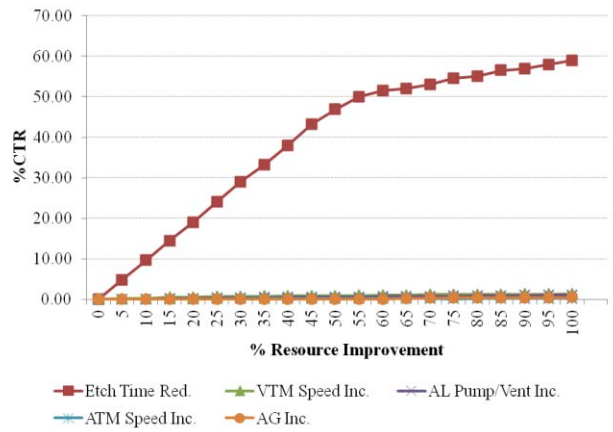

Figure 7a: Resource improvements

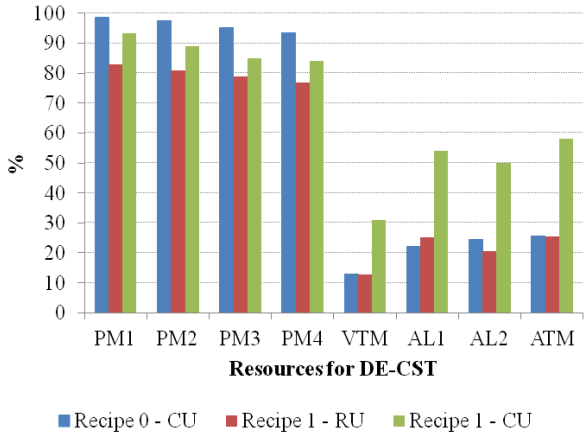

Figure 7b: Resource utilizations

Figure 7: Analyzing PM, VTM, AL, ATM, and aligner improvements and utilizations for the base case

We define a ratio, called unit improvement ratio, to identify opportunities in recipe design. Let p_i be the increase of resource performance for resource $i \in I$. Let J be the set of scenarios where $J=\{1,2\}$ and $j=1$ for "Etch Time Red." and $j=2$ for "Clean Time Red.". Let UIR_i be the unit improvement ratio for resource $i \in I$ and scenario $j \in J$ where

$$UIR_i = \frac{CTR_j}{p_i}.$$

Note that CTR_j is the cycle time increase for the scenario $j \in J$. Since UIR_i is the contribution of increasing of resource i^{th} performance for $i \in I$ to cycle time reduction for the scenario $j \in J$, the resource, which has the highest UIR, is the bottleneck, which is defined by

$$argmax\{i|UIR_i\}.$$

Figure 8a illustrates that reducing etch and cleaning times up to 45% provides almost linear reduction on the lot cycle time. However, after 45% reduction, less cycle time improvement provided per percent resource improvement. For a clean time reduction, per unit reduction up to 60% provides 0.2 reduction contributions to the lot cycle time, e.g. 5% clean time reduction reduces cycle time by 1%. The results show that 40% of the existing cleaning times can be kept for quality purposes since cleaning is required to remove particles from a chamber.

Figure 8b illustrates current utilization values for the base case when there exist 25% and 75% etch and cleaning time reduction. We observe that process chambers utilizations are reduced since ATM robot and airlocks utilizations are increased after 45% resource improvement. Thus, if the ATM robot speed and airlock pump/vent times are increased, then the lot cycle time decreases.

5 CONCLUSION

In this study, we develop a simulation model of a dry etch cluster tool based on CPN. Using the simulation model, we evaluate the performance of the dry etch cluster tool and develop new improved schedules for these tools.

We consider a frequent recipe that runs on the dry etch cluster tool for the analysis. We identify that the process chambers are the bottlenecks in the tool for the frequent recipe and lot cycle time can be significantly reduced by optimizing this recipe. We identify a threshold value for the recipe improvement when performance of ATM and airlocks impact process chambers. If the etching and cleaning times are reduced by more than 45%, then the ATM robot is the next bottleneck in the tool. In addition to the ATM robot, airlocks also have an impact to cycle time. Cleaning time reduction provides less cycle time reduc-

tion opportunity than etch and cleaning time reductions together. Cycle time can be reduced up to 14% if cleaning time is reduced up to 65%.

As a future study, we are planning to develop new simulation models based on CPN methodology for different cluster tool types.

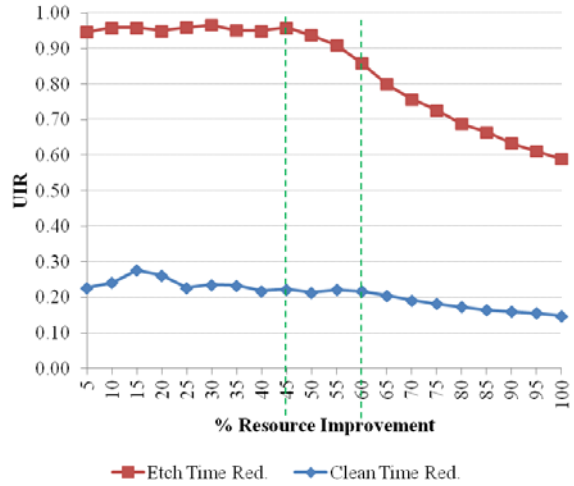

Figure 8a: UIR for recipe improvement for Recipe 0

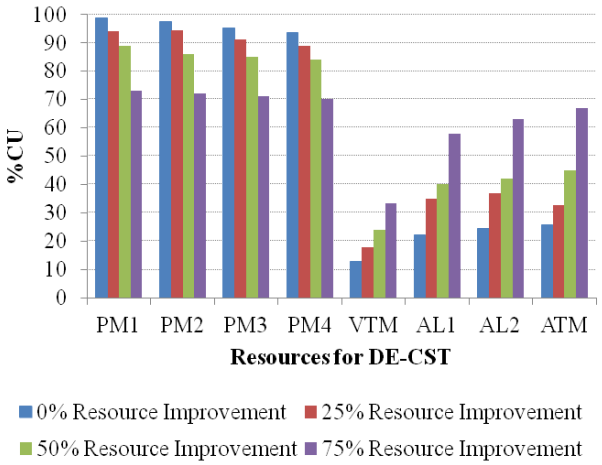

Figure 8b: Current resource utilizations for 0%, 25%, 50%, and 75% improvements for etch and clean time decrease

Figure 8: UIRs for recipe improvements and current resource utilizations for Recipe 0

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