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INTRODUCING THE VIRTUAL TIME BASED FLOW PRINCIPLE IN A HIGH-MIX LOW-VOLUME WAFER TEST FACILITY AND EXPLORING THE BEHAVIOR OF ITS KEY PERFORMANCE INDICATORS

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ABSTRACT

In modern semiconductor manufacturing and primarily in high-mix-low-volume facilities it is increasingly important to ensure throughput and machine utilization requirements are met while satisfying tight goals in object tardiness at the same time. This is especially a challenge for the field of wafer test with its natural fluctuations and uncertainties of test times. A further important objective is the lowering of the work in process (WIP) for the purposes of minimizing costs held in the system and improving production predictability. For this, the Virtual Time Based Flow Principle (VTBFP) – a partly synchronized control strategy- is investigated in this paper. Tests are performed on a complex system, which is close to reality. As a result it is shown the benefits but also the limitations of the VTBFP approach.

1 INTRODUCTION

The upcoming challenge for the semiconductor industry is to be lean and fast in all business processes, e.g. operations. Especially for mature 200 mm fabs on the "More than Moore" path in a high-mix, low-volume logic business, this is an essential need to further proceed towards the multitude of goals that have to be considered. In this context, logistic innovation becomes more and more important as complexity of products is increasing and therefore product workflows as well as cycle times grow steadily.

Current strategies to disconnect increasing cycle times from customer relevant lead times utilize storages for each product. However, applied for a wide range of product variants, this proceeding becomes uneconomical. Therefore cycle time decreasing innovations are crucial for commercial success.

A possible approach to decrease cycle time is pursuing the principle of continuous flow manufacturing, which can be achieved via the Virtual Time Based Flow Principle (VTBFP, Keil et al. 2011). Its main idea is to use only the time aspect of flow production and to logically overlay the job shop with a time based flow principle. That means the topological characteristic of the job shop with its machine layout is not changed. Preliminary investigations of VTBFP were executed in practice for minor production volumes within a wafer test environment of Infineon Technologies Dresden GmbH. These showed signif-

icant results regarding cycle time and inventory reduction. Further work attends to variability management strategies for reducing complexity, e.g. with the toolbox of lean six sigma (Eberts et al. 2012).

A further extension towards a higher proportion of production volume of the VTBFP must be evaluated prior to execution, representing an adequate risk management for both delivery and efficiency while changing the production system. This is the motivation for the application of a simulation study: Up to which proportion of the production volume is the application of the VTFTB advisable without accepting the resulting risks? As a result, the study shall provide data on key performance indicators, such as tardiness, stock and utilization.

The paper is structured as follows: In chapter 2, VTBFP is presented for a general understanding to the reader, referring to prior publications. Chapter 3 as the main part of the paper includes the description of the close-to-reality wafer test model VTFTB and its evaluation, to deduct recommendations for the real environment. Results are presented in chapter 4, followed by a summary in chapter 5.

2 THE VIRTUAL TIME BASED FLOW PRINCIPLE

Traditional manufacturing configurations are either process- or product-oriented. This leads to the differentiation of the two extremes (Miltenburg 2005): job shop manufacturing and flow production. In job shop manufacturing, tools are grouped according to their function (process-oriented). In a flow production, the installation of machines follows the product workflow (product oriented). Materials typically flow from one workstation directly to the following step. Usually, the raw process times of each production step are synchronized.

The chosen manufacturing configuration has an impact on achieving manufacturing goals including cycle time, capacity utilization, inventories and delivery reliability. Generally, within job shop manufacturing, high capacity utilization can be reached. Whereas flow production is more beneficial for minimal cycle times, low inventories as well as high delivery reliability. This depends on synchronization and balancing status of consecutive process steps . Although there are significant advantages in flow production, the established layout baseline in semiconductor production was and is undoubtedly job shop manufacturing (e. g. Chen et al. 2008; Keil et al. 2008).

However, job shop manufacturing style, which is typically assigned to make-to-order production or to small-series production, is common business practice in the gigantic mass production environments of commodity chip production. According to (Keil et al. 2008) there are three main reasons for this:

- **High speed of innovation and short product life cycles prominently reflected by Moore's law** (Moore 1965, 1975): The semiconductor market is highly dynamic. Especially the commodity market has a high frequency of technology changes. Innovation speed causes changing products and thus changing product workflows. The classical flow principle would therefor require cost intensive rearrangements of tools all the time. Further preconditions for flow production are robust production processes. This may suffer by introducing new products.
- **Economic conditions:** Since ICs are manufactured in cleanrooms, the design of new facilities is increasingly constrained by cross-contamination concerns, complex utility and chemical supply requirements. This causes rather high construction and space costs favoring compact factories. Equipment accounts for 80% of the total fab costs. Job shop allows simpler utility distributions, because the same tools with same utility distribution are installed in one area.
- **Characteristics of semiconductor production:** The fabrication of ICs is one of the most complex manufacturing processes in existence today and often requires several hundred process steps with significantly different single process times which makes synchronization of processes difficult. The product workflow is specific for every product and comprises reentrances.

Nevertheless the customers demand more and more integrated functions on a single chip. Therefore product complexity is increasing tremendously in the semiconductor industry. This results in increasing production process complexity, reflected in additional lithography layers for example. This causes longer cycle times and higher costs.

One main leverage to improve this would be a manufacturing configuration according flow production. As already introduced, the introduction of the classical flow principle is not possible in this environment. This leads to the Virtual Time Based Flow Principle (Keil et al. 2011). Generally, beside the topological aspect of flow production which comprises the installation order of machines according to the product workflow, there is a second aspect: The matching of flow times and the capacity balancing of consecutive process steps as precondition for the continuous flow of material. Consequently, the topological aspect is not mandatory for applying flow production. Therefore, the main idea is to use only the time aspect of flow production and to logically overlay the job shop with the „Virtual Time Based Flow Principle“ (VTBFP). That means the topological characteristic of the job shop is not changed.

Up to this point, there is a lack of manufacturing experience for applying only the time aspect of flow production to a topological job shop in semiconductor fabrication. This hampers the organizational innovation for changing a pure job shop system into such a flow-production-like controlled job shop. The lack of experience is further emphasized as there are only very few examples and studies which can be referred to. Although there are numerous publications for flow shops and job shops (cf. Uszoy 1994) for related concerns as e.g. their control strategy and input regulation strategies, there are rarely publications considering only the time aspect of flow control applied to a topological job shop. Evaluable data and statistics on how to implement this new production system are of similar rareness. As a consequence, no modeling approach is available, not even simulation studies.

The VTBFP is part of the approach ‘Design for Flow by 3’ which includes beside Design of Production Control for Flow also the design of Product Process of Record (POR) as well as organization for flow to reach the ideal of continuous flow manufacturing (Keil et al. 2011a). However, the focus of this paper lies on Design of Production Control for Flow with the VTBFP. Three key elements of design production controlling for flow are:

- reducing complexity of long semiconductor production flows by splitting up of the complete POR into multiple sub-sections and building flow families,
- adapt clock based production schedules iteratively to continuous flow manufacturing and, thereby
- focusing on variability management.

In a high-mix, low-volume manufacturing environment new customer oriented speed flows would have to be designed for up to hundreds of products with up to 1000 single process steps for each product. The idea is to reduce complexity through the split up of the complete POR into multiple sub-sections and build flow families. A flow family is a united chain of consecutive single process steps which are similar within different product PORs, including the following similarities:

- sections of complete POR,
- same or replacing tool types with similar process times for single process steps, and
- length and sequence are similar.

In classical approaches, e. g. Value Stream Design, it is suggested to build product families (Rother and Shook 1999) which contain the whole product flow and belonging products are of one “class”. In contrast, a flow family can contain totally different products with similar sections of POR. Once applied, complexity gets isolated within the above mentioned subsections.

These flow families are the basis for synchronized production control, which is a suitable means to manage complexity. Figure 1 shows the approach of the iterative adaption to a continuous flow. This is necessary, as the production system will be changed radically from job shop to flow production mode. Especially variability has to be regarded as a main detractor for introducing continuous flow manufacturing. The idea is to plan for each process the necessary variability buffer time individually.

Remember within the automotive industry all single process steps of an assembly line are synchronized. Therefore, a solution here is to split up each flow family into multiple so-called “Virtual Flow Units” with the same duration where several consecutive unit processes are grouped. Besides similarity there is no other rule on how to build flow families. One way could be to group them based on litho layers

(each family starting with a litho step), all with the same duration. The first flow unit is the pace maker, all following units contain as many processes (with an adequate variability buffer) until the sum of process times reaches the customer cycle time.

In a later stage fab the researched approach is successively introduced to a whole fab by merging with existing structures via several learning loops (Figure 1). Every learning loop includes a field test and at the end a pilot production phase in which the production plan is executed over a longer time period. The field tested clocked plan will continuously be modified according to latest information about both process speed calculation and made changes in surrounding processes. Over time the variability of buffer times ought to be decreased.

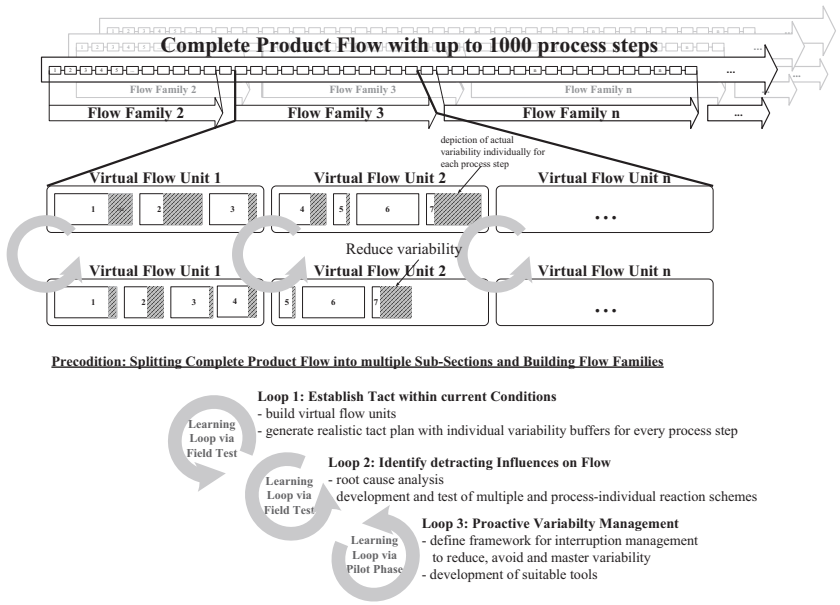

Figure 1: Approach of the iterative adaption to a continuous flow

The VTBFP principle was preliminary tested in a real wafer test environment for only 2 products. The promising results are shown in Keil et al. (2011). Further test with more than two products may be too risky in a real fab environment. Consequently, the behavior of VTBFP in the wafer test is investigated by simulation. Results should show key performance indicators and the influence to the existing manufacturing environment. The simulation model and simulation results are provided in sections 3 and 4.

3 EVALUATION OF VTBFP ON A CLOSE-TO-REALITY WAFER TEST MODEL

In this section the behavior of VTBFP is investigated by further introducing it into an previously traditional dispatching rule controlled production. For this a wafer test facility is used with its special requirements and challenges. A discrete event simulation (DES) software is used for all simulation activities. This software is the 'simcron MODELLER' (Horn et al. 2006). Amongst others, it comprises a tool command language (Tcl) interface as well as a component object model (COM) interface for interoperation purposes. Thus, Tcl was used for modeling and creating models generically. The COM interface was used for integrating spread sheets as typical data containers. As the simulation models contain stochastic process times, 100 simulation runs were performed per scenario to receive robust system information.

3.1 Wafer Test

The created model is oriented at the structure and behavior of a typical high-mix wafer test facility. With its high spreading and also high uncertainty of testing times it is of interest to improve tardiness and pre-

dictability especially in this area of semiconductor manufacturing. There are researches for dispatching rules considering process time uncertainty in relation with predictability (e.g. Lange 2010). However, the advantages of VTBFP is estimated as far more promising.

Typically, the wafer test is situated between the so-called frontend and the backend of semiconductor manufacturing. Frontend processes are typically steps such as chemical vapor deposition (CVD), physical vapor deposition (PVD), etching or lithography for structuring. The backend generally comprises all packaging processes after wafer separation (dicing) like bonding and encapsulation. The wafer test itself can be broadly departed in four sections: optical inline inspection, parameter test, functional test and optical outgoing inspection (Figure 2). Whereas the parameter test characterizes the electrical parameters, the functional test characterizes the logical behavior of the wafers' chips. The investigated wafer test area comprises up to 15 process steps per product. This is explained in more detail in section 3.2.

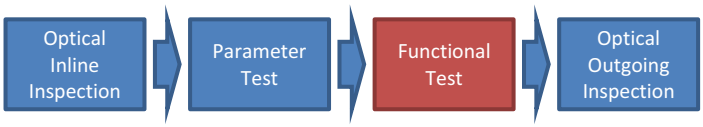

Figure 2: Schematic structure of the wafer test

Within all operations of the wafer test, the functional test operations are most time-consuming and thus crucial for optimization. At the functional test a wafer is electrically connected in a tester equipment using a probe card. For this there are pre-defined feasible combinations of approved tester, probe cards and products (Figure 3). These combination are defined by a Boolean matrix the so-called dedication matrix.

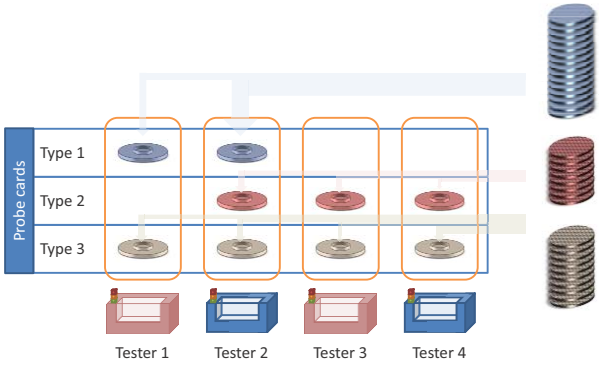

Figure 3: Tester and Probe card dedication

Several product types with individual routes and process times are tested at the investigated wafer test. Additionally, products are separated into two general priority groups. There are normal products ('N') and less important 'filling ware' products ('F'). Whereas normal products are high value products which have a high priority class, filling ware products are low value products with low priority.

3.2 Wafer Test Model

This section describes the general specifications of the model, the implementation of the VTBFP-approach as well as built scenarios for testing. The implemented model is derived from a real wafer test facility. In relation to the problem dimension of this real facility, the defined model comprises a down-scaled problem size. However, it is still considered being big enough for showing also effects for the real system.

General Specifications

The wafer test is modeled as flexible job shop with recirculation. The model comprises 14 products having different routes and process times at equal stations. Routes can have up to 15 process steps. Within these there are functional testing, furnace steps, and other steps like optical clean, logistical steps or preparation for external delivery. All these steps are implemented in the model having their own product-specific process times and specific capacities. Details of two important steps are listed below:

- **Functional test**: There is a dedication matrix for each functional test step specifying allowed combinations of products and tester. For changing the product type on a tester it is estimated to have a static setup time. In contrast to Klemmt et al. (2011), for purposes of keeping the model efficient, further setup topics as changing test programs or temperature setups are neglected as well as secondary resources (probe cards). To obtain a setup policy similar to reality, a tester processes jobs of same product until there is no other job of this product is available for a provided period. After this period the tester can change its setup to process another product.
- **Furnace step:** The furnace is modeled with unlimited capacity and has a gate interval of six hours.

Sets of process times are created out of original times for every product and step combination. So, for every lot a process time is selected randomly out of its related process time set. Product routes can have up to 15 process steps. However, the number of steps to pass is individual for every product. Figure 4 shows an example for four products extracted from the model.

Insertion

The amount of lots to be tested per week is assumed to be constant in the model. The proportion of lot amounts was determined by means of real data. Table 1 shows the proportional amount of weekly introduced products.

Table 1: Proportion of intserted objects per week

Product	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Proportion [%]	1.3	4.2	6.7	2.9	4.2	4.6	2.1	3.4	8.4	5.0	8.4	33.6	6.7	8.4

Modeling the Existing Dispatching Strategy

The control strategy of the existing manufacturing system was modeled by using the earliest due date (EDD) dispatching rule. EDD is a simple dispatching rule for achieving good results for time-related objectives such as tardiness or lateness. The traditional first-in-first-out (FIFO) dispatching approach is not used in this research since it has no effect on time-related objectives. In contrast to the more complex dispatching rule named operational due date (ODD), EDD is less effective for reentrant flows. However there are two reasons for implementing EDD instead. Firstly, compared to ODD, EDD has a better model performance by means of model calculation time. Secondly, the proportion of lots which actually have a reentrant flow is quite low. Consequently, EDD is considered as sufficient.

Modeling the Virtual Time Based Flow Principle

As introduced above, the wafer test's typical characteristic is the relatively high product-specific variation of process times. Furthermore, products usually have a wide spread in their average test times. So, a pure clocked assembly line is not to advisable. This leads to VTBFP as an intelligent product clocking approach. The modeling of the Virtual Time Based Flow Principle is mainly in the aggregation of several route operations into defined clocked segments for each product with preferably exclusive machine rights, if necessary. Figure 5 exemplarily illustrates the routing and the made segmentation for four products. For this, a segment is depicted by a shade of gray. It can be seen that segments are defined individually for

each product and that segments can contain and combine different operations. Thereby, several operations can utilize identical machines.

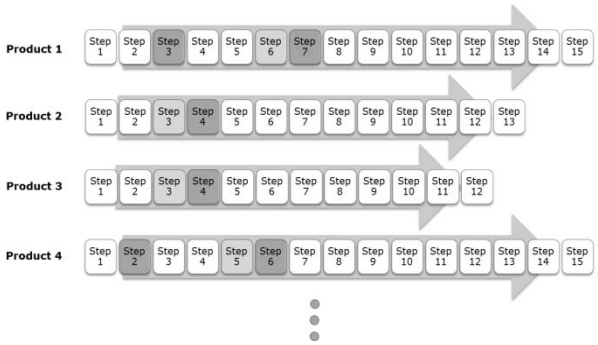

Figure 4: Possible product routes

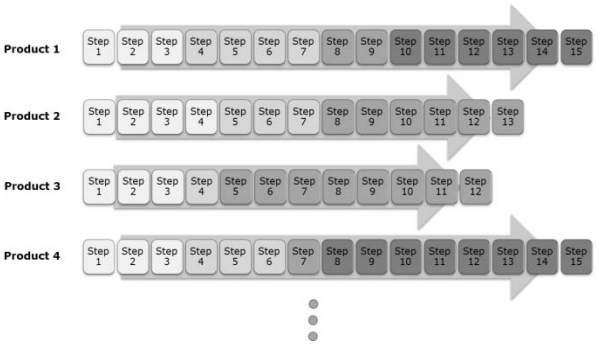

Figure 5: Possible VTBFP segmentation

For implementing clock segments as introduced in section 2, a barrier is created after the last operation of every clock segment. This is done separately for every product type. The barrier stops premature lots which are processed according to VTBFP. In the opposite case, if a lot arrives to a barrier later than the barrier due date, this lot is not blocked and free to be processed until reaching the next barrier. The barrier dates are calculated for every single job according to formula (1), where $t_j^{release}$ is the release date of a job, t_j^{clock} is the section duration per clock, j is a job out of J jobs and i is a segment out of the range from 1 to the maximum segment number I.

$$t_{i,j}^{barrier} = t_j^{release} + \frac{i * t_j^{clock}}{I}, \quad i \in [1, I], j \in J \tag{1}$$

Table 2 provides an overview about planned cycle time, number of clocked sections and durations of these sections for every product.

Table 2: Cycle time and clock attributes per product

	Planned product cycle time	Number of clocked sections	Section duration per clock		Planned product cycle time	Number of clocked sections	Section duration per clock
Product 1	1	4	0.25	Product 8	0.5	3	0.17
Product 2	0.54	3	0.18	Product 9	0.31	3	0.10
Product 3	0.43	4	0.11	Product 10	0.25	3	0.07
Product 4	0.5	4	0.13	Product 11	0.3	4	0.08
Product 5	0.67	4	0.17	Product 12	0.15	3	0.05
Product 6	0.46	4	0.12	Product 13	0.2	3	0.07
Product 7	0.5	3	0.17	Product 14	0.23	4	0.06

Since sections are defined separately for products (time and segmentation) and jobs (different starting dates and so different barriers), there is an appealingly chaotic system from a top view to the system. However, in detail there is the system of VTBFP. As a reminder there are no barriers for non-clocked lots.

Assigning exclusive machines for VTBFP products

Assigning exclusive machines for clocked products is important especially as there are variant process times. So, a simple stable synchronized workflow is not possible. Without capacity dedication this

results in changing a product, when there is free capacity even for a short time. Consequently, the number of setup rises. This can be prevented by creating dedication matrices for clocked products.

Exclusive machines for products are important for VTBFP control and only VTBFP-controlled products have those in this model. Furthermore, as the functional test operations are the most critical ones, exclusive machines are only provided for these. For purposes of keeping the model simple, there are no exclusive machines determined for remaining steps as these are less resource critical and have no setups. Exclusive machines are provided by reduced dedication matrices, where feasible tester are defined for products. Reduced dedication matrices are built for every scenario except the first scenario as defined in the following sub-section.

The first scenario uses the original dedication matrix, which defines the superset of all feasible product-tester combinations. In this case there are the least dedication restrictions and the allocation rate of 'true' is about 35%. As already introduced, only VTBFP-clocked products are tried to have exclusive machines. Remaining products retain share remaining machines. So, for the clocked products exclusive machines are calculated meaning a sufficient tester allocation for the required capacity.

The exclusive allocation of machine is still viable for low proportions of VTBFP products. However, since the overall system capacity is of course restricted, by increasing VTBFP proportion clocked products are more and more forced to share machines also considering the products' required capacity. Further information can be found in Doleschal et al. (2012).

Model scenarios

For researching the influence of introducing VTBFP, several scenarios are created. Within these scenarios, the grade of clocked products ('C') is increased. Beginning from the most important product 'Product 1' to the least important product 'Product 14'. This is shown in Table 3. Clocked products have a higher prioritization than non-clocked products. The first scenario has no clocked products and represents the initial configuration. The last scenario represents a fully VTBFP-clocked system. The period of observation is exactly one week. Thereby, the model is initially loaded and simulated for a period of five weeks. The system's behavior is solely evaluated for the third week. So, falsifications by simulation start and end effects are reduced.

Table 3: Subdivision of products for each scenario
(F..filling ware, N..normal product, C..clocked product)

Scenario	Product 1	Product 2	Product 3	Product 4	Product 5	Product 6	Product 7	Product 8	Product 9	Product 10	Product 11	Product 12	Product 13	Product 14
1	N	N	N	N	N	N	N	N	N	F	F	F	F	F
2	C	N	N	N	N	N	N	N	N	F	F	F	F	F
3	C	C	N	N	N	N	N	N	N	F	F	F	F	F
4	C	C	C	N	N	N	N	N	N	F	F	F	F	F
5	C	C	C	C	N	N	N	N	N	F	F	F	F	F
6	C	C	C	C	C	N	N	N	N	F	F	F	F	F
7	C	C	C	C	C	C	N	N	N	F	F	F	F	F
8	C	C	C	C	C	C	C	N	N	F	F	F	F	F
9	C	C	C	C	C	C	C	C	N	F	F	F	F	F
10	C	C	C	C	C	C	C	C	C	F	F	F	F	F
11	C	C	C	C	C	C	C	C	C	C	F	F	F	F
12	C	C	C	C	C	C	C	C	C	C	C	F	F	F
13	C	C	C	C	C	C	C	C	C	C	C	C	F	F
14	C	C	C	C	C	C	C	C	C	C	C	C	C	F
15	C	C	C	C	C	C	C	C	C	C	C	C	C	C

Figure 6 shows the proportion of clocked and non-clocked objects per scenario. It can be seen that introduced object amounts are not uniformly distributed. This reflects Table 1. In Figure 7 the proportion of clocked products by means of required tester capacity is displayed per scenario.

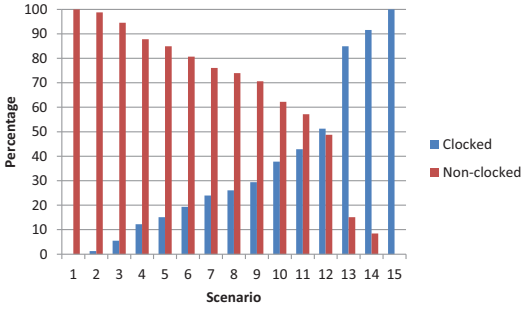

Figure 6: Clocked objects by scenario

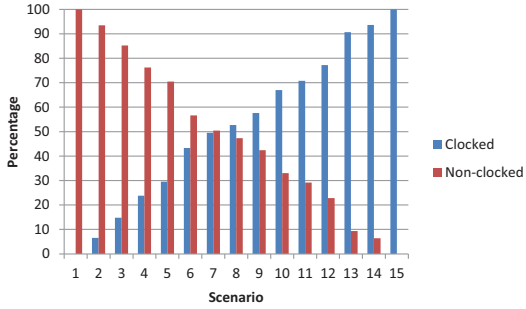

Figure 7: Clocked tester capacity by scenario

Objectives

Beside common objectives as maximizing throughput and minimizing stock, the primary objectives for the given wafer test model are lateness and tardiness. According to Pinedo (2008) the lateness L_j of a job j is defined as $L_j = C_j - d_j$, where C_j is the completion time and d_j is the due date of job j. In the same way the tardiness T_j of a job j is defined by $T_j = \max(C_j - d_j, 0)$.

4 RESULTS

This section provides results for introducing VTBFP into an EDD controlled process. Figure 8 shows the determined mean values for tardiness, lateness throughput and the number of setups over all evaluated jobs for all scenarios enlisted in Table 3. The results are normalized to those of a scenario without any clocking (scenario 1).

By introducing VTBFP for more and more products, tardiness gets increasingly smaller in the scenarios 2 till 5 and reaches values of less than 80% for scenarios 6 and 7. According to Figure 6 these scenarios equate to a clocking proportion of about 22% of the fed-in objects or according to Figure 7 about 46% of the required tester capacity. By scenario 8 and further ones, the mean tardiness values are rising again. The same is to say about lateness as it is very similar to tardiness.

For this model, similar system behavior was repeatedly observed for several runs and minor parameter changes. This means, for the regarded system there is a minimum between scenario 5 and scenario 8. For scenarios 10 and higher the system behavior tends to be undetermined meaning that small changes of input parameters may have high effect to the system behavior. So, the regarded system seems to react instable for a high degree of clocked products. The reasons for this may be first in the increasingly reduced dedication matrices of the functional testers and second in the lack of EDD controlled filling ware products, which are capable using free machine capacity more flexible.

Figure 8 also shows the determined throughput over the scenarios 1 to 15. The throughput describes the number of readily produced jobs in the period of the evaluated week. After a slight increase up to scenario 5 it decreases again reaching its minimum in scenario 15. Generally, it seems that throughput stagnates up to a certain grade of VTBFP-clocking and declines continuously for excessing it. For the regarded system, the limit for stable throughput is about 30% of clocked objects or 60% of clocked tester capacity . However throughput variations stay low. The system stock first decreases overall about 20% till scenario 5 and stays at a level for higher scenarios. Finally, the number of performed setups in the functional test steps is also depicted in Figure 8. The number of setups declines with every scenario. This effect results primarily from the reduced dedication matrices lowering the number of allowed tester per product. As a positive side-effect the time blocked by setups is so available for processing. So tester utilization is reduced by nearly 10% for the regarded system without having a lower throughput. This means a higher overall effectiveness of the system.

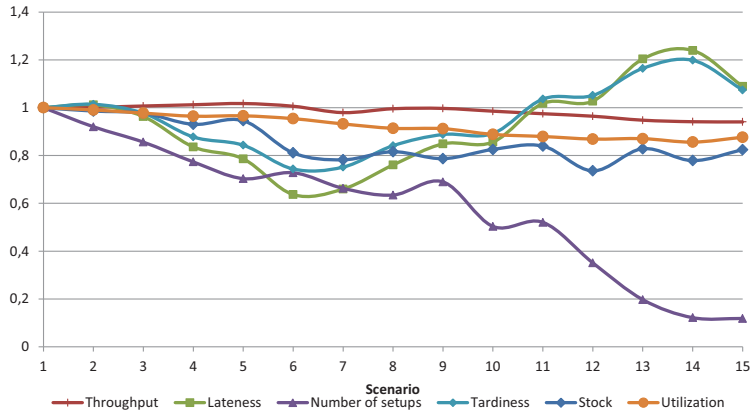

Figure 8: Results with normal dedication

Figure 9 and Figure 10 show results using differently created dedication matrices in the functional test for assigning exclusive machines for VTBFP-clocked products. Whereas results of Figure 9 are based on dedication matrices with stricter assigning of exclusive machines, these are more loose for matrices where results of Figure 10 are based on. A loose dedication means more overlapping in the dedication matrices. Results show that the system behavior is depending on the underlying creation of the dedication matrices for the functional test steps. A tighter dedication thereby creates a smaller optimal window.

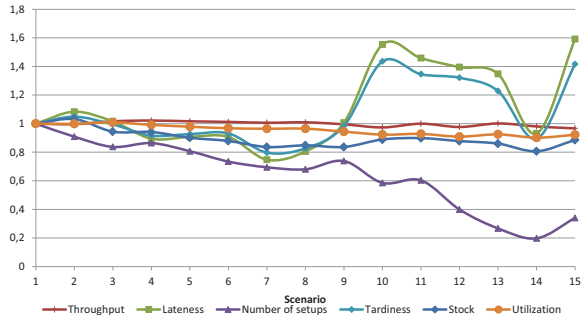

Figure 9: Results with strict dedication

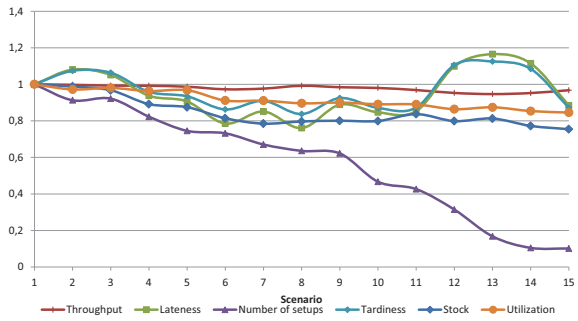

Figure 10: Results with loose dedication

Research by Doleschal et al. (2012) shows that it is generally possible to use the VTBFP-approach without assigning exclusive machines. However, due to the stochastic process times and the more balanced work flow created by VTBFP, the number of setups rises immensely. Thus, assigning exclusive machines for products is advisable. This may be less useful for process lines without any setups. Finally it can be said that the achieved results are to be considered as qualitative results. Other systems may show a different behavior and need separate considerations.

5 SUMMARY

A DES-based evaluation system was developed to research the behavior of VTBFP in an existing wafer test facility. For this purpose, a complete wafer test environment with 14 products and 15 process steps with a detailed functional test was modeled. Since the wafer test has varying process times, a pure synchronized approach is less appropriate. VTBFP provides a promising approach to ensure the main goal of the wafer test: Fulfillment of production deadlines and volumes. The behavior of VTBFP was researched with a continuous rise of the proportion of VTBFP-controlled lots. Under the given system parameters it turned out, that a partly VTBFP clocking can be advantageous. The optimum window thereby was in a domain of 15% till 30% of the introduced lots which correlates in the given system to 30% till 55% of the

tester capacity. Furthermore, setups are reduced significantly by combining VTBFP with a reduced dedication for steps having setups as the functional test in this example. However, the determination of exclusive machines has significant influence to the overall system behavior.

Next steps to be pursued are: Firstly, introducing the VTBFP/ODD mix successively into other work centers of the wafer fab and finally applying the VTBFP/ODD mix to the whole fab. Secondly, improving the model by implementing a more detailed setup according to the approach introduced in Klemmt et al. (2011) which could improve result quality. Thirdly, as this research provides a result for a single wafer test facility with its specific product mix and product volumes, the good results obtained for this setting have to be further researched on other environments to validate the results and to obtain more general findings of applying the VTBFP/ODD mix.

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