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TOWARDS A SUPPLY CHAIN SIMULATION REFERENCE MODEL FOR THE SEMICONDUCTOR INDUSTRY

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ABSTRACT

In this paper, we describe major steps to build a supply chain simulation reference model for the semiconductor industry. We start by identifying requirements for such a reference model. Then we identify the main building blocks of the model. We present a technique to deal with load-dependent cycle times in single front-end and back-end facilities and in the overall network to reduce the modeling and computational burden. The quality of this reduction technique is assessed by comparing the full model and the model with a reduced level of detail. Finally, we discuss several potential application scenarios for a simulation reference model of a semiconductor supply network.

1 INTRODUCTION

A set of very complex manufacturing processes is the heart of semiconductor manufacturing. A semiconductor chip is a highly miniaturized, integrated circuit (IC) consisting of thousands of components. Semiconductor manufacturing starts with thin discs, called wafers, made of silicon. A large number of usually identical chips can be produced on each wafer by fabricating the ICs layer by layer in a wafer fabrication facility (wafer fab). The corresponding step is referred to as the Fab step. Next, electrical tests that identify the individual dies that are likely to fail when packaged are performed in the Probe facility. An electronic map of the condition of each die is made so that only the good ones will be put into a package. The probed wafers are then sent to an Assembly facility where the good dies are put into an appropriate package. Finally, the assembled dies are sent to a test facility where they are tested in order to ensure that only good products are sent to customers.

Wafer fabrication and probe are often called the front-end and assembly and test are called the back-end. The current generation of semiconductor products often requires up to 700 unit processing steps that can take up to four months to complete.

Supply chain management (SCM) issues have become more and more important in the last decade (Chien et al. 2011). This was caused by the fact that front-end operations are often performed in highly

industrialized nations, while back-end operations are typically carried out in countries where labor rates are cheaper. In addition, today there are centers of competencies for wafer fab, probe, assembly, test, or sometimes only single process steps within the sites of companies, silicon foundries, or subcontractors. These centers of competencies speed up innovations and reduce costs, but increase the complexity of supply chain management.

The semiconductor industry is capital intensive caused by extremely expensive machines. The manufacturing process is very complex due to the reentrant flows in combination with very long cycle times and the different levels of uncertainties involved. Capacity expansions are very expensive and time-consuming. This kind of decision is based on demand forecast for the next years. Because of the rapidly changing environment, the demand is very volatile. Consequently, the forecast is rarely accurate. This characterization of semiconductor manufacturing leads to the conclusion that the semiconductor industry is an extreme field for SCM solutions from an algorithmic and also from a software point of view (Chien et al. 2011).

There are reference (simulation) models for single wafer fabs (MASM 1997), mainly developed in the Measurement and Improvement of Manufacturing Capacity (MIMAC) project (Fowler and Robinson 1995) that are used by many academic researchers working with the semiconductor industry. A second, widely used model is the MiniFab model, proposed by researchers at Intel (Spier and Kempf 1996). It is a low complexity simulation model that mimics the behavior of a wafer fab by containing reentrant process flows, batching tools, and significant sequence-dependent setup times. At the same time, such reference models for simulation are not available for supply chains in the semiconductor industry. In the present paper, we describe some initial steps to come up with a set of such reference models.

The paper is organized as follows. In the next session we describe supply chain simulation issues in the semiconductor industry. Moreover, we also discuss related literature. In Section 3, we describe the requirements for a supply chain (simulation) reference model and introduce the main building blocks of such a model. Results of simulation modeling for the base system of the supply chain reference model are presented in Section 4. Finally, we describe some possible application scenarios in Section 5.

2 SUPPLY CHAIN SIMULATION AND RELATED LITERATURE

There are many papers that deal with supply chain simulation in industries different from semiconductor manufacturing (Ingalls 1999, Schunk and Plott 2000, Chang and Makatsoris 2001, amongst others). Simulation is well accepted as a tool to support the design and control of supply chains. It is shown by Kleijnen (2005) that discrete-event simulation is an important technique to simulate the base system of supply chains, while system dynamics is used to represent the corresponding planning and control systems.

Jain et al. (1999) discuss the criticality of detailed modeling for simulating semiconductor supply chains. A supply chain model consisting of four wafer fabs and one assembly and test facility is considered. Fully detailed models are compared with reduced simulation models where only bottlenecks are modeled in detail. They conclude that fully detailed simulation models are needed. However, long computing times are reported for such models. At the same time, the modeling effort is also large. Model reduction techniques based on aggregated process flows for a single wafer fab are also discussed by Hung and Leachman (1999) in the context of iterative simulation. Because of the huge modeling effort that is needed to find appropriated aggregated routes we do not take this approach.

There is another stream of research that deals with distributed simulation to perform simulation studies for supply chains in the semiconductor industry. Lendermann et al. (2003) discuss a scenario that contains two wafer fab simulation models, one simulation model of an assembly and test facility, one warehouse, and finally one distribution center. The High-Level-Architecture (HLA) is used to couple the different simulation models, called federates. A similar approach was proposed by Chong et al. (2006). Gan et al. (2007) also use HLA in a borderless wafer fab scenario. However, because of the technical difficulties of HLA and because of the large modeling effort for each single federate we do not think that this approach is appropriate to model supply chains in the semiconductor industry.

A strict separation between planning system, control system, and base system of a supply chain is discussed in Godding, Sarjoughian, and Kempf (2003). Discrete Event System Specifications are used to model the base system of the supply chain. This approach was refined in Huang et al. (2009). Here, model predictive control is used within the planning and the control system of the supply chain. But again, only very simple supply chains are modeled and simulated.

Jain (2006) propose a conceptual framework for supply chain modeling and simulation that is based, at least in parts, on the Supply Chain Operational Reference (SCOR) model. However, it seems that the framework proposed by Jain is too generic and does not include enough specific details for simulating supply chains of the semiconductor industry.

Duarte et al. (2007) propose a compact abstraction of a single manufacturing node in a semiconductor supply network. However, the case of an entire supply chain containing different nodes is not addressed in this paper. In this paper, we will extend this approach to model entire supply networks.

We conclude that no supply chain simulation reference models, in the sense of a test-bed, are available in the semiconductor industry. However, such reference models are highly desirable because they allow to model the dynamics of the corresponding supply chains. Furthermore, such models, if publicly available on the web, would allow a fair comparison of planning algorithms proposed by different researchers without spending much effort to build a simulation model from scratch.

3 BUILDING BLOCKS OF A SIMULATION REFERENCE MODEL

In this section, we start by collecting requirements for a supply chain simulation reference model in the semiconductor industry. Then, we describe the base system used. We also discuss which parts of the planning system and control system should be included in the reference model.

3.1 Requirements of a Reference Model

In this subsection, we derive several requirements for a supply chain reference model. Of course, our point of view is influenced to a certain degree by the simulation reference models for single wafer fabs provided by the MASM Lab and by SEMATECH (MASM 1997) within the MIMAC project. We refer to these models as MIMAC models in the remainder of this paper. We derive requirements based on the insight that each supply chain consists of a planning and control system and process and a base system and process. The planning and control system is responsible for decision-making. It determines how many wafers have to start in which period of time, how much material has to be released from each inventory point, and finally where to ship the final ICs. The planning and control process is responsible for using the planning and control system. The base system consists of the resources. It is responsible for the physical flow of material through the supply network. It is possible to determine when a certain IC is completed and shipped, i.e., when customer orders are fulfilled and how much inventory is in each node of the supply network at a certain point of time using data of the base system. The base process describes how resources are used by working objects. In a certain sense, products influence the base process. Customers are responsible for orders and demand. They are considered as external entities that influence the planning and control system and at the same time the base system. We come up with the following requirements:

1. The reference model should contain a base system that is typical for a semiconductor supply network. A base system that is as simple as possible is highly desirable. It has to contain important entities that represent resources and their stochastic behavior. An appropriate level of detail has to be chosen that makes meaningful planning and control decisions possible. An appropriate modeling of load-dependent cycle times is crucial.
2. Products have to be included into the reference model to represent the base process.
3. The model should contain customers that are responsible for order generation.
4. The reference model has to contain demand information that allows planning decisions in connection with the orders of the customers. The relationship of demand and firm orders has to be incor-

porated into the reference model. Appropriate stochastic demand patterns have to be included in the reference model.

5. The reference model has to contain a simple planning and control system that determines wafer starts based on the firm orders and the given demand.
6. It is important to include a basic information and control flow into the reference model. The information flow is responsible to maintain the information status of the different decision-making entities by taking feedback from the base system and process and other decision-making entities into account, while the control flow models how planning and control instructions are communicated in the supply network.
7. Finally, the reference model has to be represented in such a way that the different end-users can easily use the simulation reference model without a specific simulation engine. ASCII files or XML data structures are appropriate to represent the model. The representation to be offered has to take the relationship between the different entities as indicated in Figure 1 into account.
8. A documentation of characteristic performance measures for the different nodes of the supply network has to be provided for end-users to check the correctness of their usage of the reference model with the default settings.

Figure 1 contains an Entity-Relationship Model (ERM) for important entities of a supply network in the semiconductor industry.

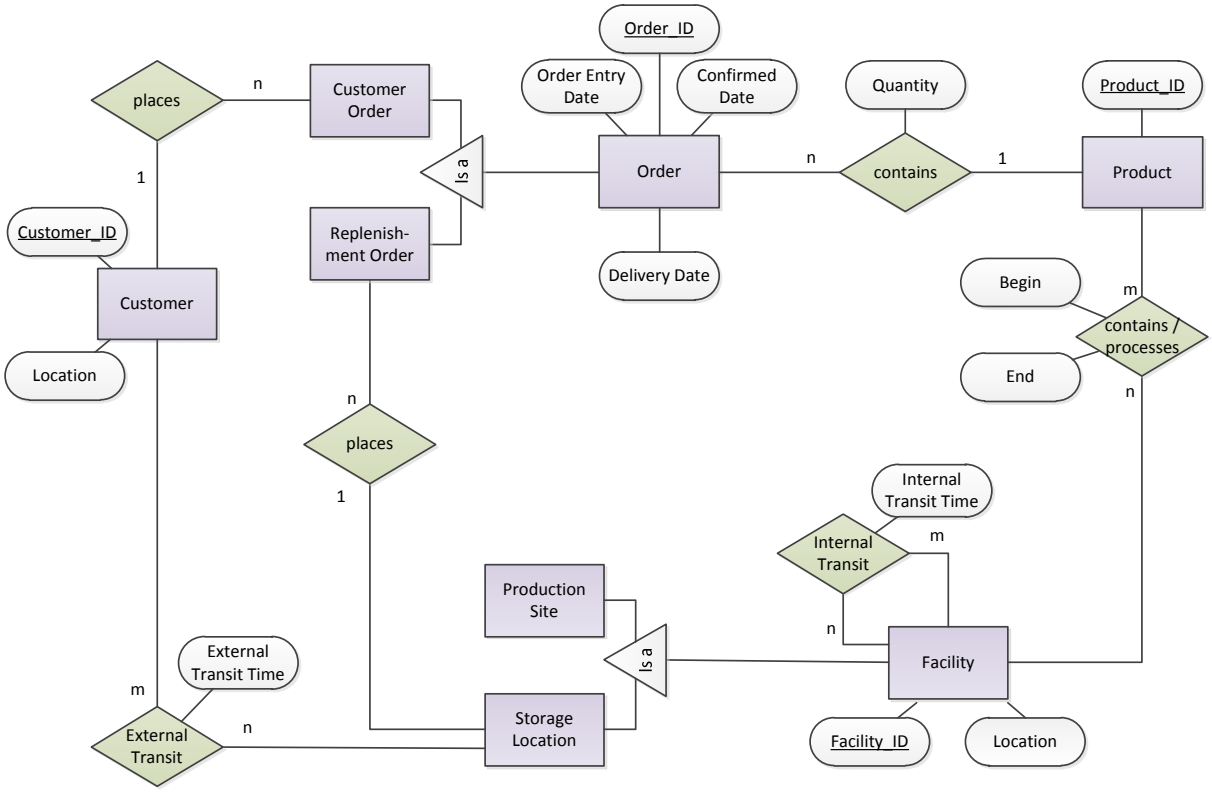

Figure 1: Important entities in a semiconductor supply chain

We continue with a description of important entities of the reference model.

3.2 Base System

We start with the base system. It represents, together with the base process, the material flow in the supply network. It contains the following entities:

- two front-end facilities (FE)
- two silicon foundries (SF)
- two die banks (DB)
- two back-end facilities (assembly and test (AT))
- two subcontractors (SC)
- two (regional) distribution centers (DC).

We decide to avoid a differentiation between wafer fabs and sort to have a low level of detail. At the same time, we do not model assembly and test using different models. Such fine-grained models are not discussed in most of the projects to create a simulation model for supply chains in the semiconductor industry (Godding, Sarjoughian, and Kempf 2003; Lendermann et al. 2003; Chong et al. 2006; Huang et al. 2009). Outsourcing options are modeled by SFs and SCs. The DBs are used to decouple front-end and back-end, whereas the DCs are between the AT facilities and the customers. Of course, customers are also part of the base system. However, we consider them as external entities that are discussed in Subsection 3.3. Suppliers of raw material are not modeled in the reference model because they are rarely a bottleneck in the semiconductor industry. We will explain the representation of capacities in the base system in more detail in Section 4.

Next, we have to include products into the reference model because they represent the base process. The reference model contains the following entities:

- two final products A and B with two stock keeping units per product
- two additional final products C and D of the same product family that have the same parent dies produced in the frond-end and packaged differently in the back-end, only one stock keeping unit is assigned to each of the final product C and D.

For each product we specify in which front-end and back-end facilities they can be processed. Furthermore, empirical cycle time distributions that depend on the load of the corresponding facility are provided for each product. We also specify a simple transportation model that includes internal and external transit times. In contrast to the cycle time, transit times are assumed to be deterministic.

3.3 External Entities

Customers have to be included into the reference model because they provide orders and more generally, demand. The following entities are used:

- one customer that is an original equipment manufacturer (OEM)
- one customer that is a distributor.

The two non-diversified final products A and B described in Subsection 3.2 are assigned to the two customers. The final products C and D are assigned to the distributor.

We assume weekly time buckets for 18 months to take the typical lifecycle of products in the semiconductor industry into account. The reference model contains the following order and demand patterns for the four products from Subsection 3.2:

- firm orders
- supply reservation
- final demand.

Firm orders are customer orders that have already been confirmed by the Order Management system. It is a binding demand that is cancellable under certain conditions. The amount of firm orders is decreasing over the time horizon. Firm orders have a default due date in the reference model. Supply reservation is an additional forecasted demand that comes either from the Sales & Operations Planning process or from the customer through a Business to Business (B2B) Electronic Data Interface (EDI). A customer forecast is a non-binding demand that can be cancelled without any restriction. It is used as a placeholder for firm orders that may arrive at a future point of time. The amount of supply reservations is increasing over the planning horizon. There is no supply reservation for the first period. The final demand states the definitive

expectation of the customer for a given time bucket. It is relevant for demand fulfillment and is equal to the firm orders of the first time bucket.

We start by generating final demand for each final product for a given demand level. It is assumed that the demand for the final products is independent. Some random noise with respect to the different quantities is taken into account. Based on the final demand, firm orders and supply reservation are determined. Forecast errors are taken into account by modeling the error as a normal distributed random variable with a prescribed mean and standard deviation. Some random noise is modeled in a similar way for the firm orders to model cancellations. Note that in addition the final demand, firm orders, and supply reservation can be based on real-world data from Infineon. A stationary demand scenario and a scenario that contains some ramping and drop down of the four products are provided in the reference model.

3.4 Planning System and Control System

In the spirit of the MIMAC models that do not provide dispatching rules for production control, we do not include any sophisticated planning and control logic in the reference model. We assume an enterprise-wide planning and control unit that provides instructions for the different FE and AT facilities. The different FE facilities do perform only short-term production planning activities. We simply take the final demand and determine lot release schedules for each time bucket by a simple backward calculation scheme taking target cycle times into account. Note that the production of parent dies for product C and D can be planned in an aggregated manner. Then the release quantities are assigned to the FE facilities and SFs using static allocation rules. Appropriate lot sizes and lots have to be determined for FE and AT facilities, respectively. Default lot sizes for AT facilities are specified in the reference model. Decisions with respect to the safety stocks for DBs and DCs are also made by the planning system. The default setting is zero safety stock.

Important performance measure values are documented in the reference model. The simple planning logic can be replaced by a more sophisticated end-user specific one. We will see, in Section 4, that a detailed simulation model of a supply network is also proposed that consists of detailed simulation models for FE and AT facilities. In this situation, performance measure values are only reported for a First-In-First-Out (FIFO) production control strategy.

3.5 Modeling of Information and Control Flows

Some simple models of the information and control flow have to be incorporated into the reference model. The firm orders are generated weekly and are sent to the enterprise-wide planning and control unit. This unit receives feedback from the AT facilities and the SCs, i.e., information on completed lots. The DCs report their shipments to the planning and control unit. Each FE facility and each SF informs the planning and control unit when wafers are completed.

Information related to DB and DC inventories is transferred to the FE and AT facilities in case of assemble-to-order and make-to-stock manufacturing strategies, respectively. Lot release schedules are sent to the FE facilities in case of a make-to-order strategy. Finally, the SFs and SCs obtain instructions related to quantities for different products to produce them. The described setting is depicted in Figure 2.

4 SIMULATION MODELING OF THE BASE SYSTEM AND PROCESS

We start by describing our approach to model single nodes in a semiconductor supply chain. Then, we extend this approach to the network situation. We describe the structure of the proposed reference models.

4.1 Modeling of Single Manufacturing Nodes

Two different approaches are used to model single manufacturing nodes. The first approach consists in considering full models of FE facilities and AT facilities. For FE facilities, we use the MIMAC-I model (MASM 1997). It consists of 73 tool groups. The products have around 240 processing steps. It contains

batch processing tools and reentrant process flows. Operators are not modeled. Moreover, we also consider a simulation model of an AT facility. It consists of 23 tool groups. Some tool groups include significant sequence-dependent setup times. Lots are split, for example, in front of the wire-bonder tool group. This model is called Back-end-I. The simulation AutoSched AP is used as simulator. We refer to these models as academic models in the remainder of this paper. However, using full simulation models leads to significant large simulation times and large effort to maintain the simulation models.

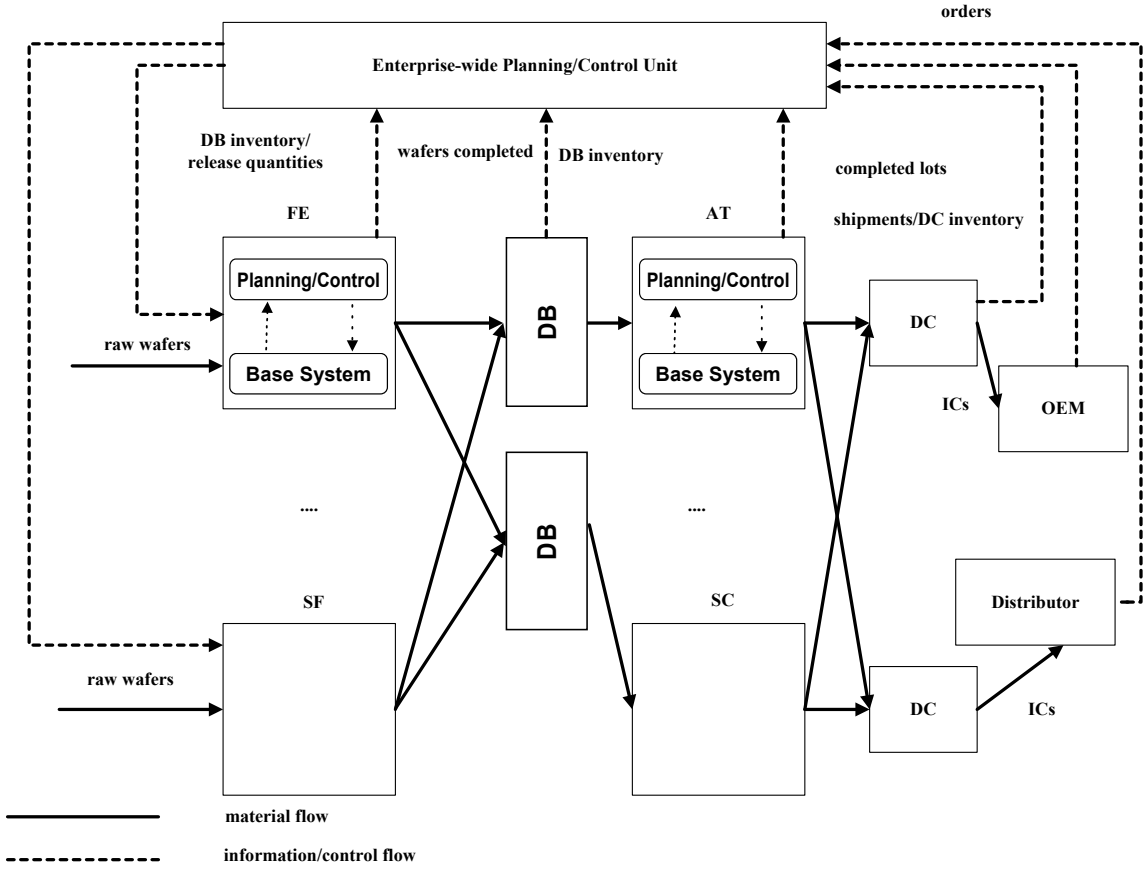

Figure 2: Flow-oriented view on the supply network

To avoid these problems, we use a model reduction approach that is inspired by Duarte et al. (2007). Our approach takes into account that cycle times are load-dependent. Therefore, we consider for a given FE or AT facility different load levels $L_i, i = 1,...,n$. A specific load level is determined by the number of released lots per time unit and leads to a certain bottleneck utilization. We assume that the bottleneck utilization for L_i is smaller than for L_{i+1}. We determine an empirical distribution of the cycle times and an empirical distribution of the time elapsed between two consecutive lot completions for a given L_i. The corresponding empirical distributions are called CT_i and TP_i. Note that TP_i represents the throughput. Consequently, each L_i is represented by a pair (TP_i, CT_i). We release lots according to TP_i by determining the corresponding inter arrival times. Each released lot obtains an individual cycle time according to a realization of the empirical distribution. Note that the pairs (TP_i, CT_i) can be easily determined using full simulation models, i.e., in case of the academic models, or real-world data. Usually three to five pairs, i.e., load levels, are enough. The procedure is shown in Figure 3.

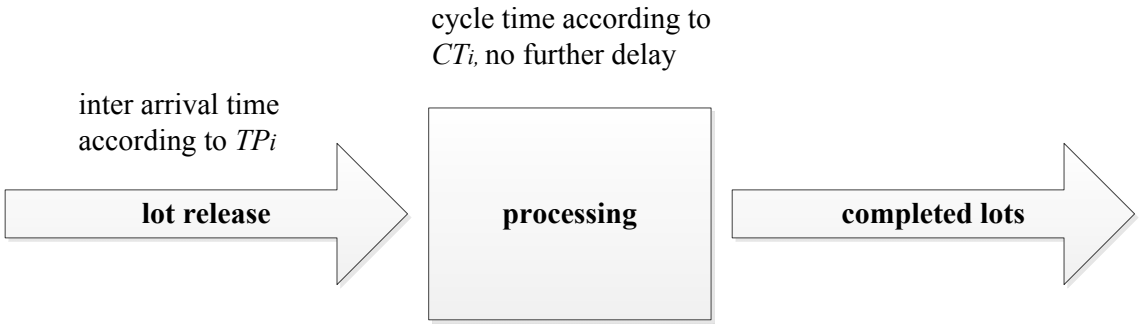

Figure 3: Basic principle of the reduced simulation model

Now we consider the situation where a load level L_j is of interest which leads to a bottleneck utilization that is between the utilization caused by L_i and L_{i+1}. Similar to the linearization approach for clearing functions proposed by Asmundsson, Rardin, and Uzsoy (2006), we interpolate linearly between CT_i and CT_{i+1} as follows

$$CT_j = \frac{E_{i+1} - E_j}{E_{i+1} - E_i} CT_i + \frac{E_j - E_i}{E_{i+1} - E_i} CT_{i+1}, \tag{1}$$

where we denote by CT_k a realization of the cycle time for L_k and by E_k the mean inter arrival time for L_k. The main difference of our approach to the approach by Duarte et al. (2007) is this linear interpolation. Duarte et al. (2007) determines an empirical cycle time distribution for a low load situation and an empirical throughput distribution for a high load. A correction term for the cycle time is calculated using Markov chains. However, it cannot be assumed that this data is always available in real-world information systems.

The approach proposed in this paper has been successfully assessed using the academic models and also real-world data from one of Infineon's FE and AT facilities, respectively.

4.2 Modeling of an Entire Manufacturing Network

Because we are interested in simulation models of supply networks, we create such models using the models for single nodes described in Subsection 4.1. In a first step, we build a simulation model of a supply network that contains two MIMAC-I FE facilities and two Back-end-I facilities. Furthermore, the full simulation model also contains two DB. Each FE lot is split into three AT lots. This full model is the base of our first reference model.

Next, we build a reduced variant of this model using the reduction technique outlined in Subsection 4.1. Two products are considered for two different load situations L_1 and L_2 for the FE facilities. Because the lot release rates in the FE facilities have an impact on the load of the AT facilities, we include DBs between the two stages to decouple them. A target Work-In-Progress (WIP) level is determined for the AT facilities based on Little's law and the target cycle time and target throughput for the AT facilities. We interpolate between the two different load situations to obtain a third load situation L_{12}. Figure 4 depicts the resulting cycle time histograms for the two products and L_2 and L_{12}, respectively. It can be seen from Figure 4 that the cycle time histogram for the full and reduced models are rather similar in case of product p_2. The simulation is run for 1000 days. This similarity is smaller for product p_1, however, the shape is still the same.

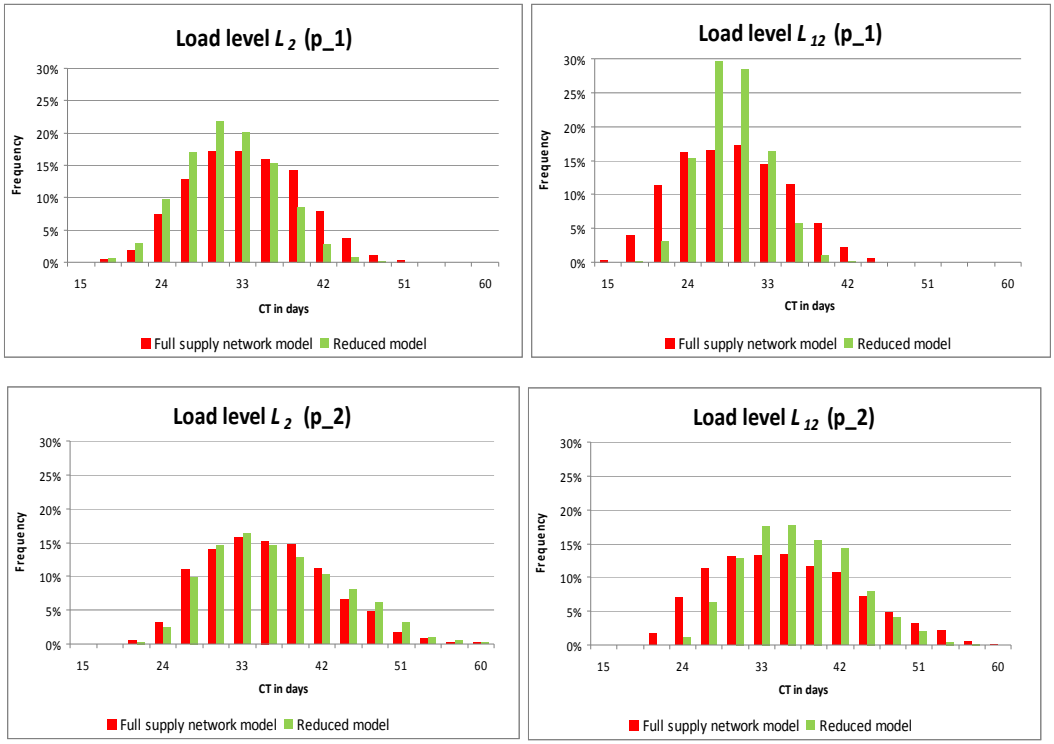

Figure 4: Comparison of a full supply network model and a reduced model

We introduce the measure

$$\overline{HD}_{abs} = \frac{\sum_{d \in D} |H_2(d) - H_1(d)|}{\sum_{d \in D} (H_1(d) + H_2(d))} \tag{2}$$

to determine the similarity between two histograms H_1 and H_2 in a more formal way. Here, we denote by $H_i(d)$ the frequency of the category d. We obtain $\overline{HD}_{abs} = 0.2607$ for p_1 and $\overline{HD}_{abs} = 0.1701$ for p_2.

Statistics for the corresponding cycle time distributions are summarized in Table 1. We can see that the variance is lower in the reduced model due to the linear interpolation according to expression (1).

Table 1: Statistics for cycle time distribution obtained by the full and reduced simulation models

Compare	Product p_1		Product p_2	
	full model	reduced model	full model	reduced model
minimum	12.917	16.756	18.139	21.839
maximum	44.559	40.217	61.022	55.775
median	27.324	27.149	33.791	35.044
mean	27.508	27.314	34.425	35.429
variance	35.418	13.469	63.404	37.289
coefficient of variation	0.216	0.134	0.231	0.172

A similar supply reference model will be provided that is based on real-world data from Infineon. It includes two FE facilities and two AT facilities as described in Subsection 3.2.

5 POTENTIAL APPLICATION SCENARIOS

The first application scenario is related to the assessment of master planning approaches for supply networks in semiconductor manufacturing. Here, for given firm orders and supply reservation, production quantities for each FE and AT facility of the supply network are determined. The planning approaches are used within a rolling horizon setting. Simulation can be applied to represent the base system and the base process. The performance of the proposed approaches can be assessed by appropriate robustness measures using a stochastic demand and a stochastic base system. Heuristics for a simplified master planning problem including several FE facilities and the corresponding simulation-based performance assessment are discussed by Ponsignon and Mönch (2010). The approach by Hung and Leachman (1999) is applied to reduce the simulation models of the full FE facilities. When the framework is used, the simple planning logic described in Subsection 3.4 has to be replaced by a more sophisticated master planning approach. Generally, long and medium term planning approaches for entire semiconductor networks are rarely discussed in the literature. One reason for this situation might be the huge modeling effort to create homegrown simulation models from scratch to apply these approaches in a rolling horizon setting.

The second application scenario deals with make-to-stock, assemble-to-order, and make-to-order decisions (see Sun et al. 2010 for a related study). Here, the default due dates of orders have to be changed in the reference models to model the fact that, for make-to-stock and assemble-to-order, final products can have a tight due date, and appropriate safety stocks have to be added to the reference model to verify the effect on delivery reliability to the customers.

Note that the two discussed application scenarios can be based on the reference models that do not include full simulation models of the FE and AT facilities because production control decisions, i.e., dispatching or scheduling decisions for lots on tools, are not important. Hence, the fast simulation of the reduced models offers some advantage. Using the full supply network reference model makes sense when the interaction between the production planning and production control strategy should be studied in detail.

6 CONCLUSIONS AND FUTURE RESEARCH

In this paper, we discussed important steps towards the ultimate goal of having reference models for supply chains in the semiconductor industry. After determining requirements for simulation reference models, we identified the main building blocks of such models. Then, we presented an approach to obtain a supply chain network as a set of reduced simulation models using an approach similar to the abstraction method proposed by Duarte et al. (2007). We demonstrated that this approach works well for both academic models and models based on data from the industry, respectively. Finally, we discussed some potential applications scenarios for the reference models.

There are some directions for future research. First of all, we have to complete the proposed simulation reference models by adding more details with respect to modeling customers, i.e., order generation, forecast, product ramp-ups and drop-downs, and by modeling inventory points. Furthermore, more research is needed to adjust the models to different product mix situations because so far we assumed only very simple situations with a small number of products. Finally, it is highly desirable to demonstrate the impact of the reference models by using them for the application scenarios described in Section 5.

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REFERENCES

Asmundsson, J., R. L. Rardin, and R. Uzsoy. 2006. "Tractable Nonlinear Production Planning Models for Semiconductor Wafer Fabrication Facilities." *IEEE Transactions on Semiconductor Manufacturing* 19(1):95-111.

Chang, Y., and H. Makatsoris. 2001. "Supply Chain Modeling Using Simulation." *International Journal of Simulation* 2(1): 24-30.

Chien, C.-F., S. Dauzere-Peres, H. Ehm, J. W. Fowler, Z. Jiang, S. Krishnaswamy, L. Mönch, and R. Uzsoy. 2011. "Modeling and Analysis of Semiconductor Manufacturing in a Shrinking World: Challenges and Successes." *European Journal of Industrial Engineering* 5(3):254-271.

Chong, C.-S., P. Lendermann, B. P. Gan, B. Duarte, J. W. Fowler, and T. Callarman. 2006. "Development and Analysis of a Customer Demand Driven Semiconductor Supply Chain Model Using the High Level Architecture (HLA)." *International Journal of Simulation and Process Modelling* 2(3/4):210-221.

Duarte, B., J. W. Fowler, K. Knutson, E. Gel, and D. Shunk. 2007. "A Compact Abstraction of Manufacturing Nodes in a Supply Network." *International Journal of Simulation and Process Modelling* 3(3):115-126.

Fowler, J. W., and J. Robinson. 1995. "Measurement and Improvement of Manufacturing Capacity (MIMAC) Final Report." Technology Transfer #95062861A-TR, SEMATECH.

Gan, B.-P., M. Liow, A. K. Gupta, P. Lendermann, S. J. Turner, and X. G. Wang. 2007. "Analysis of a Borderless Fab Using Interoperating AutoSched AP Models." *International Journal of Production Research* 45(3):675-697.

Godding, G., H. S. Sarjoughian, and K. G. Kempf. 2003. "Semiconductor Supply Network Simulation." In *Proceedings of the 2003 Winter Simulation Conference*, edited by S. E. Chick, P. J. Sanchez, D. M. Ferrin, and D. J. Morrice, 1593-1601. Piscataway, New Jersey: Institute of Electrical and Electronics Engineers, Inc.

Huang, D., H. S. Sarjoughian, G. W. Godding, D. E. Rivera, K. G. Kempf, and H. Mittelmann. 2009. "Simulation of Semiconductor Manufacturing Supply-Chain Systems With DEVS, MPC, and KIB." *IEEE Transactions on Semiconductor Manufacturing* 22:164-174.

Hung, Y.-F., and R. C. Leachman. 1999. "Reduced Simulation Models of Wafer Fabrication Facilities." *International Journal of Production Research* 37(12): 2685–2701.

Ingalls, R. 1998. "The Value of Simulation in Modeling Supply Chains." In *Proceedings of the 1998 Winter Simulation Conference*, edited by D. J. Medeiros, E. F. Watson, J. S. Carson, and M. S. Manivannan, 1371-1375. Piscataway, New Jersey: Institute of Electrical and Electronics Engineers, Inc.

Jain, S., C.-C. Lim, B.-P. Gan, and Y.-H. Low. 1999. "Criticality of Detailed Modeling in Semiconductor Supply Chain Simulation." In *Proceedings of the 1999 Winter Simulation Conference*, edited by P. A. Farrington, H. B. Nembhard, D. T. Sturrock, and G. W. Evans, 888-896. Piscataway, New Jersey: Institute of Electrical and Electronics Engineers, Inc.

Jain, S. 2006. "A Conceptual Framework for Supply Chain Modelling and Simulation." *International Journal of Simulation and Process Modelling* 2(3/4):154-167.

Kleijnen, J. P. C. 2005. "Supply Chain Simulation Tools and Techniques: A Survey." *International Journal of Simulation and Process Modelling* 1(1/2): 85 -89.

Lendermann, P., N. Julka, B.-P. Gan, D. Chen, L. F. McGinnis, and J. P. McGinnis. 2003. "Distributed Supply Chain Simulation as a Decision Support Tool for the Semiconductor Industry." *Simulation: Transactions of the Society for Modeling and Simulation* 79(3):126-38.

MASM 1997. Test Data Sets. Accessed June 1, 2011. http://www.sim.uni-hannover.de/~svs/wise0809/pds/masmlab/factory_datasets/.

Ponsignon, T., and L. Mönch. 2010. "Architecture for Simulation-Based Performance Assessment of Planning Approaches in Semiconductor Manufacturing." In *Proceedings of the 2010 Winter Sim-*

ulation Conference, edited by B. Johansson, S. Jain, J. Montoya-Torres, J. Hugan, and E. Yücesan, 341-349. Piscataway, New Jersey: Institute of Electrical and Electronics Engineers, Inc.

Schunk, D., and B. Plott. 2000. "Using Simulation to Analyze Supply Chains." In *Proceedings of the 2000 Winter Simulation Conference*, edited by J. A. Joines, R. R. Barton, K. Kang, and P. A. Fishwick, 1095-1100. Piscataway, New Jersey: Institute of Electrical and Electronics Engineers, Inc.

Spier, J., and K. G. Kempf. 1996. "Simulation of Emergent Behavior in Manufacturing Systems." In *Proceedings of the IEEE/SEMI Advanced Semiconductor Manufacturing Conference*, 90-94.

Sun, Y., D. L. Shunk, J. W. Fowler, and E. S. Gel. 2010. "Strategic Factor-Driven Supply Chain Design for Semiconductors." *California Journal of Operations Management* 8(1):31-43.

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