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ON THE FIDELITY OF THE AX+B EQUIPMENT MODEL FOR CLUSTERED PHOTOLITHOGRAPHY SCANNERS IN FAB-LEVEL SIMULATION

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ABSTRACT

Linear and affine ($Ax+B$) models are commonly used to model equipment throughput in semiconductor wafer fabricator simulations. We endeavor to assess the quality of such models for the prohibitively expensive clustered photolithography scanner. The simulations demonstrate that such models are of varying quality. They can exhibit significant deviation from the system behavior when the simulation parameters, such as product mix and wafers per lot, change from those used to create the models. The error in throughput can range from about 4% to 60% as the number of wafers per lot varies from 24 to 1. These errors are of particular relevance for studies that consider a change to small lot sizes and high mix, as is predicted in the 450 mm era.

1 INTRODUCTION

The anticipated environment for the era of 450 mm semiconductor wafer fabrication will feature a reduction in the number of wafers per lot and a consequent increase in the frequency of setups. Due to these factors, equipment throughput is expected to be significantly less than is possible under ideal operation. To assess the feasibility and cost of future fabricators, fab-level simulation is one key tool employed. However, as we will demonstrate, the equipment models used in such simulations to predict the throughput of key tool sets can have substantial error. A more accurate model with acceptable computational tractability should be considered for certain applications.

State-of-the-art 300 mm semiconductor wafer fabricators can cost on the order of US$5 billion to construct (Forum 2011). Future 450 mm wafer fabs are expected to cost much more. Due to the large costs of such facilities, the design of and changes to production control policies, release rates, equipment capacity and maintenance policies should be carefully studied. Full fabricator simulation is an important tool to help guide such business and operation decisions; see, for example, (Fandel and Wright 2008) and (Pillai 2008).

Equipment models are an essential component of full fabricator simulation, as they play a primary role in dictating fab throughput and cycle time. There are many models available for use. Linear models are commonly used in supply chain planning and some equipment purchase decisions. Affine models, more popularly known as $Ax+B$ models, are more expressive than the simple linear models and provide better predictions of equipment performance (Radloff, Abravanel, Rhoads, Steeg, van der Meulen, and Petraitis 2009). They were first proposed by SEMATECH and are used in many commercial fab-wide simulation softwares.

The simplified linear and affine models may be considered *aggregation models* as they subsume the underlying details of the equipment behavior into a few aggregate parameters (e.g., the A and B). Other aggregation models have been proposed and/or studied in (Brooks and Tobias 2000, Rose 2000, Johnson, Fowler, and Mackulak 2005, Rose 2007, Hopp and Spearman 2008) and (Lefeber and Armbruster 2011). Aggregation models based on effective process times and of increasing capabilities were proposed for

semiconductor equipment in (Jacobs, Etman, van Campen, and Rooda 2001, Jacobs, Etman, van Campen, and Rooda 2003, Jacobs, van Bakel, Etman, and Rooda 2006, Johnson, Fowler, and Mackulak 2005, Kock, Etman, and Rooda 2008, Kock, Wullems, Etman, Adan, Nijsse, and Rooda 2008, Veeger, Etman, van Herk, and Rooda 2010a, Veeger, Etman, van Herk, and Rooda 2010b) and (Veeger, Etman, Lefeber, Adan, van Herk, and Rooda 2011).

Flow line models have more recently been suggested for modeling clustered photolithography tools (CPTs) and multi cluster tools in (Morrison 2009, Morrison 2010, Morrison 2011). They are more expressive and have been claimed to well predict CPT behavior, as they use more explicit (less aggregate) models, but suffer from greater computational requirements. There are more detailed models that include features such as control of wafer handling robots. Examples include Petri net models. However, their applicability to large scale fab-wide simulation is limited precisely due to their additional detail; computational demands are too great.

A distinction between the aggregate models, such as the $Ax+B$ model, and the flow line models are that the aggregate model parameters are determined, or "trained", based on a specific set of input data. That is, the training is reflective of a particular instance of wafers per lot and mix (though there may be many different wafers per lot in the sample, the sample does not change). As such, an aggregate model may suffer inaccuracy when the model is used in a situation outside of the training data. Flow line models, on the other hand, allow and account for changes in product mix and wafers per lot.

In this paper we endeavor to determine how much accuracy is sacrificed by the $Ax+B$ models in comparison to their flow line counterparts for clustered photolithography tools (CPTs). To answer this question, we use deterministic flow line models with redundant modules as our baseline model for CPT simulation. We consider this model to be a sufficient surrogate for the full simulation of a CPT (which might include several wafer handling robots) since a CPT is essentially a flow line in which multiple robots transport the wafers. Flow line models have been claimed to give throughput predictions within 1% of data measured from equipment logs in (Morrison 2011). Such fidelity is adequate for our purposes.

Affine models are more expressive than linear models and have largely been accepted by the industry as sufficient. In fact, they are quite good models for many classes of tools. However, as we will demonstrate, clustered photolithography tools are not one of them. This is in some sense surprising. As affine models can be constructed to allow lot dependent constant offsets B, that is, $B(i)$ is a function of the lot index i, they are fairly flexible at predicting the implications of lot specific first wafer delay. In addition, we develop an extension of the basic idea of the affine model to allow the constant offset B to depend on both the previous lot $i-1$ and the current lot i, that is, $B(i-1,i)$. This extension will allow greater modeling capability to address changes in setup frequency. Though affine models are generally considered expressive enough, as we will demonstrate, even extending the basic B to $B(i,i-1)$ is not enough to describe the behavior of clustered photolithography tools. The presence of an internal wafer buffer of significant size creates non-linear dependence on lot size and setup frequency that is not accounted for by the affine models or its extensions.

Simulations comparing various models are conducted. We develop the models based on what we consider typical for 300 mm wafer fabs. That is, we assume there are on average twenty four wafers per lot and setups faced by one in six lots. The simulations demonstrate that as we consider smaller lot sizes and/or an increase in the setup frequency, the affine models give increasingly poor predictions of throughput ranging from about 4% to 60% error. Smaller lot sizes and increased setup frequency are anticipated in 450 mm wafer fabs. In particular, lot sizes of 3, 5 and 10 wafers have been recommended and/or discussed in (Pettinato and Pillai 2005) and (Kondo 2006).

To our knowledge, linear and affine models are at the heart of all fab-level simulations and industry planning engines. They are based on average throughput behavior inferred from 300 mm fabs; they do not incorporate the significant non-linear behavior of such tools as clustered photolithography tools (CPTs). As a consequence, the average values for throughput used in such models may have substantial errors for CPTs; our simulations suggest 46.6%, 37.2% and 21.7% average throughput error for 3, 5 and 10 wafers

per lot. These linear and affine models are typically used to predict the economic viability of 450 mm semiconductor wafer fabricators and assess the implications of increased product diversity and lot size reduction (for customization or hot lots) in modern 300 mm fabs.

A key reason that affine models of CPTs suffer this error is that the affine models must be constructed based on some data. That data is typically scaled from existing equipment data. However, there are nonlinear effects that grow worse as the lot sizes change and cannot be predicted well in advance. The flow line models naturally address this nonlinearity; they explicitly model it. The simulations also suggest that much smaller errors would be obtained if the estimates for 450 mm wafer fab average tool throughput values are based on values obtained by the consideration of only those lots and setup circumstances that closely mimic those anticipated in the 450 mm wafer fab era. This is because an affine model such as the Ax+B model can provide quite good accuracy when the situation to be studied does not vary too much from the training data in terms of wafers per lot and setup frequency. Otherwise, the errors can be quite large. Still, the parameters for the affine models must be chosen based on fixed product mix and wafer size assumptions. They will give errors when studying other parameter values that diverge from the assumptions.

As a result of our study, we suggest that the more detailed flow line models be considered for select tools such as CPTs in fab-level simulation. While there is a computational burden associated with the additional detail, it should be quite reasonable if used on a limited number of tools.

The paper is organized as follows. In Section 2, we review linear, affine and flow line models for semiconductor manufacturing equipment simulation. In Section 3, we conduct a detailed simulation study to compare the models. Concluding remarks are presented in Section 4.

2 CLASSES OF EQUIPMENT MODELS

There are a vast array of equipment models available for use in fab-wide discrete-event simulation. However, two are by far the most prevalent: linear and affine models. The flow line model has recently been suggested and claimed to give very accurate predictions of tool throughput. In this section, we will review the essence of these models. Throughout we will use T_i^{CT}, T_i^{TT} and W_i to denote the cycle time of lot i on a tool, throughput time of lot i on a tool and wafers in lot i, respectively. The cycle time $T_i^{CT} := C_i - S_i$, where C_i and S_i denote the time instant at which lot i completes production and begins production on the tool, respectively. The throughput time $T_i^{CT} := min\{CT_i, C_i - C_{i-1}\}$. It is a measure of the amount of a tool's available time that is consumed by the the production of lot i. The so-called *parallel factor* ((Butler and Matthews 2001, van der Eerden, Saenger, Walbrick, Niesing, and Schuurhuis 2006, Morrison and Martin 2007a, Morrison and Martin 2007b)) may be defined as $||_i = T_i^{CT}/T_i^{TT}$. For the average values we will write $\overline{T}^{CT}$, $\overline{T}^{TT}$ and $\overline{||}$. Similarly for $\overline{W}$. The average $\overline{||}$ measures the number of lots or parts thereof that are on the tool at a given time. For given $\overline{T}^{TT}$ and $\overline{W}$ obtained as an average over all lots processed on the tool in a given time frame, the throughput capability of the tool is typically calculated as $\lambda^* := A \cdot \overline{W}/\overline{T}^{TT}$, where A is the average tool availability (proportion of time the tool is available to conduct production).

2.1 Linear Models

Linear models of lot throughput time with respect to the number of wafers in a lot are widespread in supply chain management and capacity planning; see, for example, (Denton, Forrest, and Milne 2006, Bermon and Hood 1999). This is in part due to the use of linear programming and mixed-integer linear programming for such efforts. Such a model has the form

$$T_i^{TT} = A_i \cdot W_i, \tag{1}$$

where A_i has units of time/wafer. For simplicity, the A_i may be replaced with an average value A.

2.2 Affine Models

Affine models of lot throughput time with respect to the number of wafers attempt to address the non-linearities associated with equipment setups and the the so-called *first wafer delay*; see, for example (Schmidt, Weigang, and Rose 2006, Radloff, Abravanel, Rhoads, Steeg, van der Meulen, and Petraitis 2009). Such a model has the general form

$$T_i^{TT} = A_i \cdot (W_i - 1) + B_i, \tag{2}$$

where A_i and B_i have units of time/wafer and time, respectively. The model predicts that the throughput time of a lot on a tool is essentially an affine function of the number of wafers in the lot. The idea for the model can be seen by considering the serial processing circular cluster tool in the left of Figure 1. The tool consists of four process chambers that each wafer must visit in turn. The load locks for two lots are shown at the bottom of the figure. When the tool is empty, the first wafer of the next lot must receive service from each process in turn before it is complete. Thus, there is a first wafer delay before the first completed wafer exits the tool; this is the B_i in the model. Thereafter, one completed wafer exits the tool every bottleneck process duration; this duration is the A_i. The right of Figure 1 shows the form of the cycle time as a function of wafers per lot. For simplicity, the model may use a fixed $B_i := B$ for all lots i obtained by averaging over data in the sample studied.

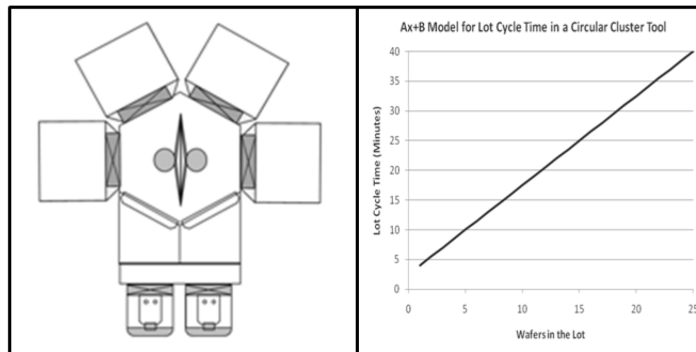

Figure 1: A serial cluster tool and throughput time model.

Though the affine model, commonly referred to as the $Ax + B$ model in the semiconductor wafer manufacturing industry, has served admirably for many years, its simplicity limits applicability to CPTs (which often feature a pre-scan track, post-scan track, photolithography scanner and wafer buffers between them). As such, one of the key tool sets that dictate fabricator capacity may not be well modeled in fab-level simulations. In particular, for a CPT with a wafer buffer prior to (or after) the scanner and facing a significant number of setups on the track and/or reticle changes:

- There is no analytic method to obtain the B values for the Ax+B model; and
- Empirically obtained values for B only give correct values for the exact situation for which the data was collected.

These problems are particularly difficult when assessing changes to photolithography capacity, determining the capacity loss caused by running small lot sizes, or determining the number of CPTs required for a 450 mm wafer fab.

2.3 Flow Line Models

Flow line models have recently been proposed to address some of the difficulties associated with using affine models for cluster photolithography tools (CPTs). They consist of a sequence of M processes which must be conducted on arriving wafers in turn; refer to Figure 2. There the processes are labeled $P_1,\ldots,P_6$. Each process is provided by a number of equivalent process modules; a wafer can receive processing from any of them. We use R_j to denote the number of modules devoted to process P_j. In Figure 2, $M = 6$ and $R_3 = 2$. Wafers advance from one process to the next as soon as a module catering to that process is available. We refer to this as opportunistic advancement. Wafers are processed in a first come first serve order. There are no wafer transport robots and we thus equivalently assume that such robots are fast (relative to process times), plentiful and not pathologically controlled (that is they, do not deadlock or reduce the rate of wafer flow).

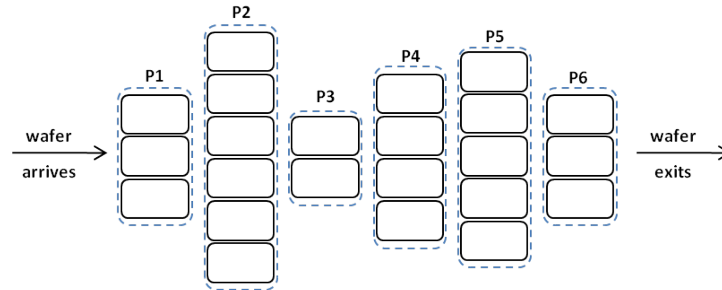

Figure 2: A flow line consists of a sequence of processes.

Let X_w^j, a_w and τ_w^j denote the start time of wafer w in process P_j, arrival time of wafer w (it is the same as the lot arrival time) and deterministic process time of wafer w in process P_j. The dynamics of such a flow line are given by the *elementary evolution equations*

$$X_w^1 = \max\{a_w, X_{w-R_1}^2\}, \tag{3}$$

$$X_w^j = \max\{X_w^{j-1} + \tau_w^{j-1}, X_{w-R_j}^{j+1}\}, \tag{4}$$

$$X_w^M = \max\{X_w^{M-1} + \tau_w^{M-1}, X_{w-R_M}^j + \tau_{w-R_M}^j\}, \tag{5}$$

with initial conditions $X_0^j = -\infty$. As is discussed in the classic paper (Avi-Itzhak 1965), a wafer buffer can be equivalently modeled as a process with zero process time. Thus, we do not distinguish between buffer slots and processes.

Clearly, this model is significantly more detailed than the linear or affine models. It is this detail that allows it to accurately describe the complexities of CPTs. The caveat is that flow line models require more data to populate and require additional computation. It is not surprising that there is thus a trade off between model accuracy and computation/ease of implementation.

3 CPT SIMULATION

To explore the effectiveness of affine models for describing the throughput and cycle time behavior of clustered photolithography tools (CPTs), we conduct simulations of a typical CPT. We use the flow line model described in the prequel as a surrogate for a full CPT simulation. As mentioned in (Morrison 2011), such as model has been observed to provide throughput predictions within 1% of actual data from CPT tool logs. We thus consider the flow line model as accurate enough to represent a CPT. Note that a key reason flow line models give good accuracy for CPTs is that, aside from the wafer transport robots, they

include many details of wafer advancement in such tools. The dismissal of the robots is possible since there are numerous robots and they do not limit throughput in such tools. A flow line model for a CPT is depicted in Figure 3.

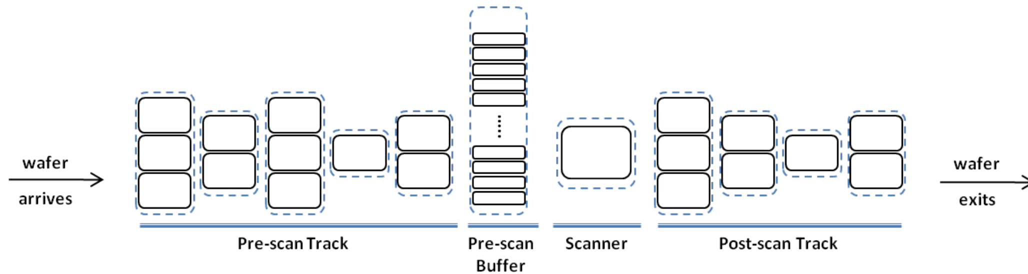

Figure 3: CPTs can be well modeled by flow lines.

We will study the CPT whose parameters are provided in Table 1. For simplicity, we will consider three classes of lots and let $\tau_w^j(k)$ denote the process time of a wafer of class k in process P_j. There, process P_6 represents the 24 wafer buffer just prior to the scanner which provides process P_7. The process times are given in Table 2. While the data is fictitious, it is inspired by real values from production CPTs in the industry.

3.1 System Description

For all simulations conducted, we will simulate for $18,000$ lots and 10 replications. To remove transients, we ignore the data from the first $3,000$ lots. As our primary interest is in assessing how well affine models predict tool throughput capacity, we assume that lots arrive to the tools in a just in time (JIT) manner. That is, there are always lots waiting to receive processing. The class of a lot is random (we use a Markov chain model to determine how the class changes from lot to lot). We will consider two average train sizes $T = 3$ and $T = 6$. The train size is the average number of lots between a change in lot class. When changing from one lot class to another, a setup on the pre-scan track is required. This setup begins once all wafers of the prior lot have vacated the pre-scan track (processes P_1 through P_5) and entered the pre-scan buffer (process P_6). The pre-scan track then remains empty while conducting the setup for a uniformly distributed duration from $[240,420]$ seconds. Once the setup is complete, wafers from the new lot enter process P_1. During this time, the wafers in the buffer will continue to feed the bottleneck scan process P_7. When the first wafer of the new lot arrives to the scan process P_7, a reticle alignment is required of uniformly distributed duration from $[120,300]$. We do not consider the post-scan track setup as we have observed that real tools conduct this setup more quickly than the reticle alignment (this is why we do not include a post-scan wafer buffer).

This model is used as our baseline CPT. With $W_i := W = 24$ for all lots, and average train size of $T = 6$ lots between setups, we generate data for T_i^{TT}. This data is then used to determine the A_i and B_i in our affine model. That is, just as is done in the industry, we train our affine model using manufacturing data consistent with the way the fab is currently operating. The resulting model is detailed in Tables 3 and 4. There, we have generalized the concept of the affine model as much as possible so that it has a greater chance of predicting accurately. That is, the A and B values depend on the class of the current lot and the class of the lot just prior to it. We denote these parameters as $A_{k(i),k(i-1)}$ and $B_{k(i),k(i-1)}$, where we use $k(i)$ to denote the class of lot i. Since the bottleneck process time in process P_7 does not change after the first wafer, there is no dependency on the previous lot (thus $A_{k(i),k(i-1)}$ has constant rows). However, the first wafer exit times from the tool are different if the prior wafer is of a different class.

Table 1: Parameters for our flow line model of a CPT.

M	R_1	R_2	R_3	R_4	R_5	R_6	R_7	R_8	R_9	R_{10}	R_{11}	R_{12}
12	2	3	1	2	1	24	1	1	3	2	1	3

Table 2: Process data for the three classes of lots.

Class k	$\tau_w^1(k)$	$\tau_w^2(k)$	$\tau_w^3(k)$	$\tau_w^4(k)$	$\tau_w^5(k)$	$\tau_w^6(k)$
1	98	135	32	104	38	0
2	100	138	37	90	36	0
3	92	129	39	96	34	0
Class k	$\tau_w^7(k)$	$\tau_w^8(k)$	$\tau_w^9(k)$	$\tau_w^{10}(k)$	$\tau_w^{11}(k)$	$\tau_w^{12}(k)$
1	65	26	147	90	28	93
2	60	29	129	80	33	90
3	55	23	138	70	34	99

Table 3: Parameters for the generalized affine model of our CPT: $A_{k(i),k(i-1)}$.

$A_{k(i),k(i-1)}$	$k(i-1)=1$	$k(i-1)=2$	$k(i-1)=3$
$k(i)=1$	65	65	65
$k(i)=2$	60	60	60
$k(i)=3$	55	55	55

Table 4: Parameters for the generalized affine model of our CPT: $B_{k(i),k(i-1)}$.

$B_{k(i),k(i-1)}$	$k(i-1)=1$	$k(i-1)=2$	$k(i-1)=3$
$k(i)=1$	65	298.69	296.40
$k(i)=2$	245.87	60	267.54
$k(i)=3$	244.71	267.60	55

Table 5: Percent error in $\overline{T}^{TT}$ predictions by the generalized affine model.

Wafers Per Lot	1	2	3	4	5	6	7	8
Affine Model: $\%\overline{T}_{TT}$Error	-60.0	-52.1	-46.4	-41.1	-37.2	-32.7	-29.9	-26.5
Wafers Per Lot	9	10	11	12	13	14	15	16
Affine Model: $\%\overline{T}_{TT}$Error	-24.6	-21.7	-19.9	-17.8	-16.6	-14.4	-13.5	-11.8
Wafers Per Lot	17	18	19	20	21	22	23	24
Affine Model: $\%\overline{T}_{TT}$Error	-10.8	-9.4	-8.7	-7.4	-6.7	-5.7	-5.4	-4.2

3.2 Simulation Results

The affine model gives quite good predictions of the CPTs average throughput time $\overline{T}_{TT}$ when we do not change the manufacturing environment. This is completely expected since the model was constructed (trained) based on equivalent data. However, to test the response of the affine model to changes in the frequency of setups we change the train size to $T = 3$. With the new train size, we then change the number of wafers per lot W. Figure 4 depicts the average throughput time per lot as we vary the wafers per lot. (The throughput time is equivalently called the time between lot exits from the tool.) There, for $W = 24$, the error caused by the shift to $T = 3$ from $T = 6$ is only -4.2%. However, as the number of wafers changes the generalized affine model loses fidelity. Table 5 provides the % error in the generalized affine model when compared with the CPT flow line simulation. Since the throughput capacity of the CPT is essentially the inverse of this $\overline{T}_{TT}$, the capacity model is significantly in error as well. In particular, since the $\overline{T}_{TT}$ is less than the actual value (negative % error), the throughput capacity predicted by the affine model is greater than the actual throughput of the tool.

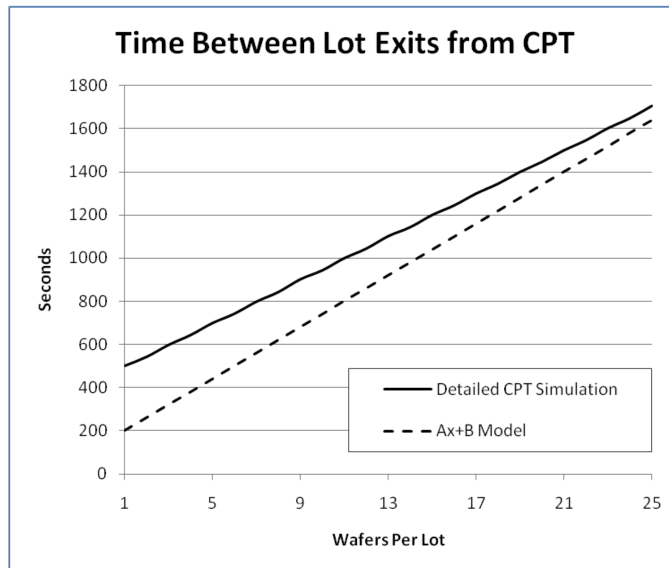

Figure 4: A flow line consists of a sequence of processes.

4 CONCLUDING REMARKS

Affine models of equipment cycle time and throughput time are a staple of state-of-the-art simulation models for fab-level simulation. Such models are often used to estimate the significance of changes in mix, wafers per lot or a transition to 450 mm wafer diameters. However, for clustered photolithography tools (CPTs), they are not sufficiently expressive to describe the tool behavior when the assumptions used to create the affine model are violated. To assess the magnitude of these errors, we conducted simulations of a typical CPT using fairly detailed flow line models. We trained our affine model with an average of six lots between setups and 24 wafers per lot. It was observed that changes to the train size and number of wafers per lot can result in throughput time predictions that are increasingly in error as the parameters diverge from their training values. In particular, as the number of wafers per lot reduced from 24 to 1, the throughput time errors grew from about 4% to 60%. The errors were about 30% for 12 wafer lots. These errors can imply significant over predictions of CPT throughput capacity.

There are numerous possible future directions and questions. It would be of interest to study a greater variety of tools and parameter values. Can a simpler model that captures the essence of the flow line models be developed? How much additional computation is required when using such models in a full fabricator simulation? Ideally, it would be greatly insightful to compare two industry full-fab simulations side by side with the only difference being the class of model used for the CPTs.

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