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SIMULATING CONVEYOR-BASED AMHS LAYOUT CONFIGURATIONS IN SMALL WAFER LOT MANUFACTURING ENVIRONMENTS

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ABSTRACT

Automated material handling systems (AMHS) using conveyors have been recently proposed as a technology option for next generation wafer fabrication facilities. This technology seems to provide an increasing capacity for moving and storing wafers in a continuous flow transport environment. The goal of this research is to design and test conveyor-based AMHS configurations, which include turntables and storage areas near the processing equipment. Simulation models were developed in AutoMod to determine the best conveyor layout, with emphasis in comparing centralized versus distributed storage systems. The AMHS factors under study comprise the number, location, and capacity of the storage areas. Simulation results show that the distributed storage approach provides improved performance; however, these systems require more capital investment than that needed for the centralized storage approach.

1 INTRODUCTION

International SEMATECH Manufacturing Initiative (ISMI) launched the Next Generation Factory (NGF) program; this program aims to decrease the costs of the wafer processing facility (fab) by 30% and lower the wafer cycle time by 50% (ISMI 2011). NGF's emphasis is on improving the fab and equipment productivity by implementing small lot manufacturing environments, improving predictive and preventive equipment maintenance capabilities, enhancing equipment quality assurance, reducing equipment setups, improving flow of wafers to equipment, among others projects.

Small lot manufacturing (SLM) is a semiconductor manufacturing initiative that seeks to reduce the lot sizes from 25 wafers to 12 wafers per processing batch. SLM has shown significant improvements in the cycle time of high-product mix fabs (Bass and Wright 2008). However, the automated material handling system (AMHS) is a potential factor that will inhibit the productivity of such environments. For the purposes of the AMHS, each processing batch of 12 wafers is transported inside a front opening unified pod (FOUP), referred herein as a wafer carrier. Studies have shown that vehicle-based AMHS may become too congested in 12-wafer-lot systems due to the increased move requirements and high dependence on stockers (Jimenez et al. 2010).

Conveyor-based AMHS are emerging as an alternative to existing vehicle-based AMHS for providing high-speed, high-throughput deliveries (Pettinato and Pillai 2005). Due to the higher availability of conveyors, the delivery time variability will be lower than in vehicle-based AMHS. The main reason is that in a vehicle-based system, a wafer carrier waits for a considerable amount of time at the tool port to

be picked up by an unloaded, unassigned vehicle. These waiting times are highly variable due to the high levels of congestion that most vehicles encounter while traveling in the AMHS tracks. By contrast, the conveyor-based AMHS has a continuous flow that virtually eliminates such waiting times. That is, a wafer carrier leaves the tool port faster and at a near constant speed once a space is allocated in the conveyor track. Another benefit of conveyor-based AMHS is that it provides higher storage capabilities near the processing equipment, therefore reducing the need for large stocker units and increasing the flow rate of wafers into the processing equipment (Nazzal and El-Nashar 2008). For more detailed discussion of the advantages of using conveyors as the primary AMHS technology in future 450mm wafer fabs, the reader is referred to Pettinato and Pillai (2005).

According to Pillai (2006), there is a lack of work regarding the evaluation of the continuous flow transporters' (CFT's) peak transport capabilities. However, the literature presents several proposed layout configurations based on conveyors (i.e., distributed storage layout and centralized storage layout). The distributed storage approach consists of one central conveyor loop in the bay and several mini storage areas that extend around each processing tool, thus providing additional buffer zones at the tool level. These buffer zones are nonetheless small, as they can accommodate a few number of wafer carriers. The centralized storage approach consists of one central conveyor loop in the bay and one storage area in the center of the bay. The capacity of the central storage area is large enough to accommodate the storage needs of the tools assigned to the bay. In both cases, such conveyor layouts will allow for decreased congestion; however, it is unknown whether the centralized or distributed storage will be more efficient.

With this in mind, the purpose of this paper is to use discrete event simulation in order to model and analyze distributed and centralized conveyor storage systems. To accomplish this purpose, conveyor-based models based off the ISMI 12-wafer-lot fab (Jimenez et al. 2010) were developed in AutoMod v. 12.1. The simulation models allowed the study of the interactions that occur between the processing equipment and the AMHS by estimating critical performance metrics, such as wafer cycle time, WIP, delivery time, equipment utilization, and conveyor utilization.

The remaining part of this paper is as follows. Section 2 presents the related literature review. Section 3 describes the characteristics of the 300mm virtual fab under study, and describes in detail the distributed and centralized storage conveyor configurations. Section 4 presents our experimental design and provides a comparative study of the two proposed systems. Section 5 summarizes the conclusions of this study and explains our future work.

2 LITERATURE REVIEW

Recent published work attempts to design AMHS for SLM-based fabs, as well as for upcoming 450mm wafer fabs. Glüer (2003) discussed the importance of optimizing AMHS operations due to the high amount of move transaction observed in megafabs. Pillai (2006) indicated that the next generation transport systems must have higher transport capabilities than existing vehicle-based solutions. Zimmerhackl et al. (2007) investigated the effects of SLM on factory performance. Their analysis resulted in 23% reduction in cycle time. The authors identified the need for further studies on AMHS operation, equipment front-end design, and FOUP handling scenarios. Jimenez et al. (2010) analyzed the AMHS factors that constrain SLM environments, which consisted of the number of vehicles, the number of stockers, the amount of AMHS track, and the vehicle control policies. These factors were optimized in order to account for the increased WIP levels in the 12-wafer-lot systems.

Pettinato and Pillai (2005) proposed the use of continuous flow transporters (CFT) as the primary AMHS for 450 mm wafer fabs since this technology provides high transport capacity, short and predictable delivery times, and low costs. CFT can also provide local buffering of wafers near the processing tool, possibly reducing the need for large stockers or larger process tool footprints. Several publications are concerned with analytical models for closed-loop conveyors with multiple stations. For instance, Nazzal et al. (2008) created an analytical model to analyze conveyor-based AMHS with turntables. The analytical models estimate the WIP levels in the conveyor at different turntable and conveyor speeds. Johnson et al. (2009) developed a greedy heuristic to optimize the configuration of an

interbay conveyor-based AMHS. The optimal layout was found through an analytical model of a conveyor-based AMHS with turntables and crossovers. Such analytical model estimated optimal delivery times and number of carriers in the AMHS as a function of the layout configuration.

3 DESCRIPTION OF SYSTEM AND CORRESPONDING SIMULATION MODELS

3.1 12-Wafer-Lot Virtual Fab

Texas State University-San Marcos and International SEMATECH Manufacturing Initiative (ISMI) worked together to develop a 300 mm virtual manufacturing fab; Linked Capacity/AMHS models were developed in AutoSched AP and AutoMod for this purpose. These models were concepts driven by SEMATECH'S Factory for Small Lot Manufacturing.

Three different technologies make up the AutoSched AP model infrastructure including 32nm, 45nm, and 65nm, where 65 nm is represented by three process flows with a total of 8, 9, and 10 metal levels. Fab capacity is set to 30,000 wafer starts per month (wspm) for product wafers and 4,500 wspm for test wafers. Each wafer requires approximately 500 to 700 processing steps. There are 54 different workstations and about 700 tools.

The AutoMod models have the following characteristics:

- Bays are arranged along a central spine layout with an inner loop and two outer loops. The layout dimensions are 230 ft. in length by 780 ft. in width. Each bay is 110 ft. in length with 10 ft. between interbay tracks. Also, each bay is separated by 35 ft. with 5 ft. between the two tracks in that bay.
- The fab contains 38 bays, each with a maximum capacity of 24 tools. The tools have a finite capacity. Figure 1 visually represents the tool distribution organized by bay and tool position.
- The AMHS performs tool-to-tool moves and tool-to-stocker/stocker-to-tool moves.
- All tracks of the AMHS are unidirectional.

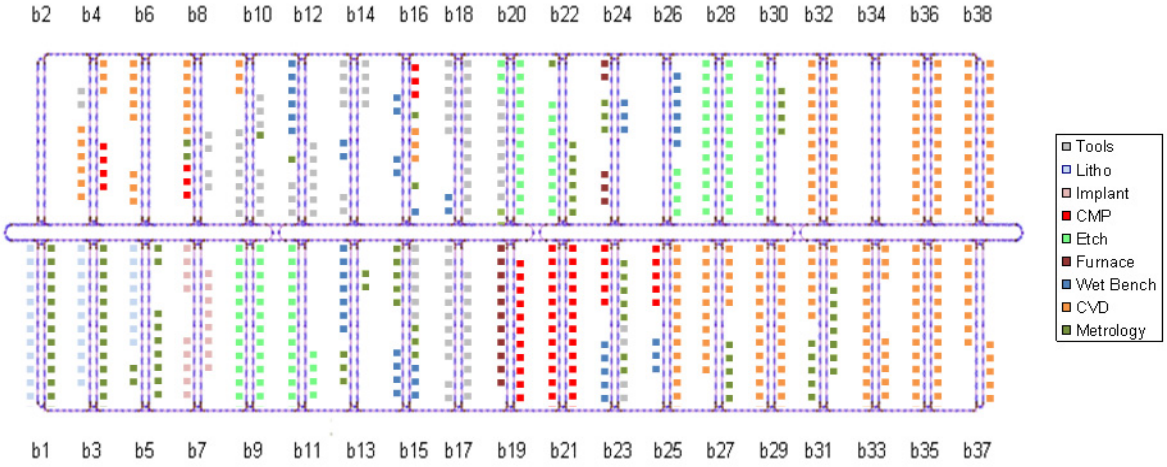

Figure 1: Tool distribution in the 300mm virtual fab model

In this paper, a focus on one single bay will give the insight needed for conveyors without the complexity of modeling and running an entire wafer fab; simulation run time for an entire wafer fab can exceed 48 hours. To properly model the variations in traffic experienced in each bay, a high throughput and a low throughput bay were both created. The specifications for each bay were designed to mimic as best as possible the model developed by Texas State and ISMI. Both models were developed in AutoMod and all attributes prescribed in ASAP were incorporated into these models.

The system consists of unidirectional conveyor tracks having two speeds with turntables at each intersection that allow for a change in the wafer carrier's orientation. Each turntable can accommodate one wafer carrier at a time. Turntable logic in rotation is governed by an AutoMod process that produces a 90 degree rotation at the arrival of a carrier and returns to the original orientation after the carrier has departed; the turn-table rotational time is varied for the purposes of our experiments, which are further discussed in Section 4.

In order to develop the high and low throughput carrier routes, data was extracted from the route defined in the ASAP model developed by Texas State and ISMI. Bay selection was based on two factors: (1) number of carriers arriving at each bay, and (2) bays with tools of utilization greater than 80%. The high throughput bay was required to have a high number of carriers arriving at the bay. Furthermore, a bay with photolithography tools was part of the selection criteria of the high throughput bay due to the status of these tools as bottlenecks in the fab, as well as the high capital costs of this tool family. The high throughput bay is based on bay b7, as shown in Figure 1, whereas the low throughput bay is based on bay b38 in Figure 1. The average carriers processed in bays b7 and b38 are 113 moves per hour and 23 moves per hour, respectively.

The high throughput bay selected consisted of three tools in a given route: photolithography, inspection, and measurement. The processing route for each wafer consisted of photolithography, measurement, and inspection with deterministic processing times of 18 minutes, 1 minute, and 1 minute respectively. Each bay contained seven photolithography tools, one measurement tool, and one inspection tool. The low throughput bay selected consisted of twenty-four copper vapor deposition inspection (CVD) tools. The processing route for each wafer consisted of two consecutive processing steps, each with a deterministic processing time of 15 minutes.

Each processing tool in the system has an internal queue to store wafer carriers. This internal queue provides faster access of wafer into the processing area of the tool. The capacity of these queues ranges between 3-4 wafer carriers per tool. The release rate of wafer carriers into the bay was based on an assumption of 85% utilization at each processing tool, and calculated using Little's Law (Hopp & Spearman 2008). Therefore, one wafer carrier is released exponentially every 3 minutes for both the high and the low throughput bay systems. If a wafer carrier arrives to a tool and the tool's internal queue is at full capacity, the carrier will be sent to the conveyor's buffer storage system. In this study, two buffer storage systems are analyzed and are described in sections 3.2 and 3.3.

The current models lack the tool to conveyor interface. Currently the logic allows for a time delay to represent the interaction between the tool and conveyor. To increase precision of collected data, an ASAP model should be integrated with AutoMod to better represent the variability of tool processing times, preventative maintenance, down times, and conveyor-to-tool interaction.

3.2 Distributed Storage System

The distributed buffer model design is an extension of the illustrated models proposed by Johnson et al. (2009). The distributed storage system has storage areas allocated at each tool; these buffers are located in Figure 2. The buffer capacity is 8 wafer carriers. The system ensures carriers are not delayed by constantly checking tool availability. There are two tracks. The first track serves as primary storage to the tool and the second track serves as a feeder system into the primary storage buffer. Additional tracks can be added if more storage is needed at the tool. The buffer system follows the assumption of zero bumping of carriers, and is operated under the rule of first come first served. The conveyors will move the incoming carriers to the target tool port. Once the internal queue capacity for a tool has reached its maximum capacity, the carriers will travel into the distributed tool buffer. The layout configuration using the distributed storage approach contains 1,460 feet of conveyor track and 148 turntables. Throughout the model there are smart checkpoints that will determine if there is capacity at the tool.

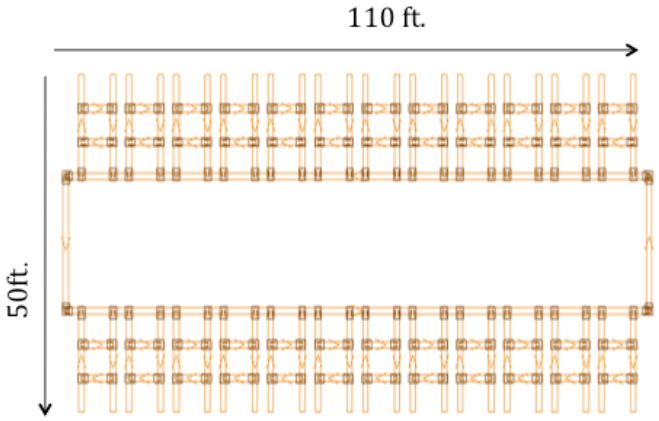

Figure 2: Layout for the Distributed Storage System

3.3 Centralized Storage System

The central buffer model design was adapted from a design proposed by Middlesex Industries (2011). The central storage system consists of two buffer loops located in the middle of the bay. The buffer layout is represented in Figure 3. The upper loop services the top twelve tools in the bay. Similarly, the lower loop services the remaining tools. Each of these loops moves wafer carriers in a unidirectional clockwise direction; carriers are in constant motion. Carriers entering and leaving the buffer system are backlogged and retrieved on a first come first served basis. There are two entry points and two exit points in each buffer loops, each controlled by smart points. The purposes of the smart points are to constantly check whether a particular load passing through is required by a tool. Once the tool queue has space available, the carrier will be called from the corresponding central storage loop, and then it will travel to the assigned tool to complete its processing step. The layout configuration using the centralized storage approach contains 900 feet of conveyor track and 73 turntables.

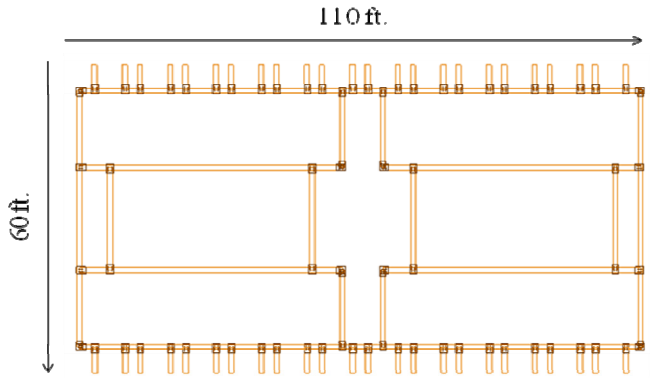

Figure 3: Layout for the Centralized Storage System

4 SUMMARY OF SIMULATION RESULTS

This section presents an evaluation of two conveyor-based AMHS configurations, one using the distributed storage system and the other using the centralized storage system. The design of the simulation experiments defines critical factors affecting the performance of the conveyor. These factors include the number of moves (Factor A), turntable speed (Factor B), conveyor speed (Factor C), and buffer storage system (Factor D). High and low levels of each factor were assigned to best represent the possible con-

veyor configurations, if implemented. A total of 16 different factor combinations resulted from the experimental design. Thus, a simulation model was developed for each factor combination. Table 1 provides a summary of the factors and their respective levels for each simulation scenario.

Table 1: Summary of experimental factors and factor levels

Model	Factor A: Number of Moves	Factor B: Turntable Speed (sec.)	Factor C: Conveyor Speed (sec.)	Factor D: Buffer Storage System
A	Low	5	.305	Central
B	Low	7	.305	Central
C	Low	5	1.000	Central
D	Low	7	1.000	Central
E	Low	5	.305	Distributed
F	Low	7	.305	Distributed
G	Low	5	1.000	Distributed
H	Low	7	1.000	Distributed
I	High	5	.305	Central
J	High	7	.305	Central
K	High	5	1.000	Central
L	High	7	1.000	Central
M	High	5	.305	Distributed
N	High	7	.305	Distributed
O	High	5	1.000	Distributed
P	High	7	1.000	Distributed

Ten replications of the experiment were produced for each model. Each run was simulated for 72 days; the first 2 days were the warm-up period to allow the performance statistics to reach steady state. The performance metrics that were collected from the simulation experiments include:

- Average cycle time, which accounts for the total time that a carrier spends in the bay.
- Average work in process (WIP), which is the average number of carriers in the bay at any given time.
- Conveyor utilization, which is defined as the average number of carriers on the conveyor track per length of track (centralized storage system = 900 ft., distributed storage system = 1460 ft.).
- Tool utilization, which measures the actual amount of time that a tool is used against the total amount of time that the tool is available.
- Average number of carriers in buffer system.
- Average number of carriers in internal tool queue, which is the average number of carriers in any tool queue at any given time.

The corresponding simulation results are shown in Table 2. Results showed that the high throughput bay produced tool utilizations of approximately 86%. The corresponding average cycle time in the high-throughput case ranges from 5433 to 7067 seconds, and the average WIP ranges from 30.3 to 39.4 wafer carriers. The turntable speed (Factor B) did not affect average cycle time. However, increasing the conveyor speed (Factor C) decreased average cycle time from 6956 to 5481. The conveyor utilization was between 0.68% and 2.32%. The average number of carriers in the tool was between 2.61 and 2.70, and the average number of loads in the buffer was between 5.65 and 6.61.

Table 2: Summary of simulation results

Model	Cycle Time, in seconds	WIP, in 12 wafer lot carriers	Conveyor Utilization	Tool Utilization	Average Number of Carriers in Buffer	Average Number of Carriers in Tool
A	3595	19.8	1.10%	41.3%	0.20	0.54
B	3610	19.9	1.11%	41.3%	0.20	0.54
C	2821	15.5	0.37%	41.3%	0.14	0.55
D	2835	15.6	0.40%	41.3%	0.14	0.55
E	3980	21.9	0.61%	41.3%	0.14	0.55
F	4000	22.0	0.62%	41.3%	0.14	0.55
G	2949	16.2	0.21%	41.3%	0.14	0.55
H	2969	16.4	0.22%	41.3%	0.14	0.55
I	7038	39.2	2.30%	85.9%	6.58	2.61
J	7067	39.4	2.32%	85.9%	6.61	2.61
K	5508	30.7	1.28%	85.8%	6.48	2.67
L	5523	30.8	1.29%	85.9%	6.45	2.67
M	6844	38.1	1.23%	85.9%	5.66	2.70
N	6876	38.3	1.24%	85.9%	5.65	2.70
O	5433	30.3	0.68%	85.9%	5.73	2.70
P	5461	30.4	0.69%	85.9%	5.73	2.70

The average cycle time in low-throughput bays ranges from 2821.41 to 4000.49 seconds, whereas the average WIP ranges between 15.53 to 22.03 carriers. The low-throughput bay produced a tool utilization of 41%. The conveyor utilization in the low-throughput bay was between 0.21% and 1.11%. The average number of carriers in the tool was between approximately 0.55, and the average number of carriers in the buffer was between 0.14 and 0.20.

The distributed storage system layout provides slightly lower average cycle times and WIP than the centralized storage system layout. In the low-throughput scenario, the difference in the average cycle time and WIP were 259 seconds and 1.4 carriers, respectively. In the high-throughput scenario, the difference in the average cycle time and WIP were 131 seconds and 0.6 wafer carriers, respectively. Due to the amount of wafers that it processes, for a low-throughput bay the conveyor storage areas were practically not used. The average number of wafer carriers per buffer in the low-throughput bay was approximately 0.14 carriers for the distributed storage system and 0.17 carriers for the centralized storage system. On the other hand, the average number of wafer carriers per buffer in the high-throughput bay was approximately 5.69 carriers for the distributed storage system and 6.53 carriers for the centralized storage system. However, according to our statistical analysis, the differences between these two layouts were insignificant (using a statistical significance level of 0.05).

5 CONCLUSIONS AND FUTURE WORK

In this paper, two conveyor-based AMHS configurations are proposed for wafer fabs with small lot manufacturing environments. Such conveyor-based AMHS will help control the WIP and reduce cycle times. The storage systems studied in both configurations did not show significant differences in average cycle time and WIP. However, from a cost perspective, the centralized storage system would be more beneficial since it utilizes fewer tracks and turntables. The distributed storage requires an additional 560 ft. in conveyor length and double the number of turntables in relation to the centralized storage system. In both

cases, faster conveyor speed netted lower cycle times and lower WIP. The analysis into the cost benefit should be studied through Cost of Ownership (COO) methodology to determine the actual economic benefits.

Future work includes the integration of the Automod model with AutoShed AP. The purpose of this integration is to create a more precise model that will include actual wafer process times, as well as the interaction between tools and conveyor stations.

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