Proceedings of the 2010 Winter Simulation Conference
B. Johansson, S. Jain, J. Montoya-Torres, J. Hugan, and E. Yücesan, eds.

SIMULATION BASED FAB SCHEDULER: SEEPLAN®

Keyhoon Ko
Seock K. Yoo
Byung H. Kim

VMS Solutions Co., Ltd.
Hanshin S-MECA 611, Gwanpyeong, Yuseong-gu
Daejeon, 305-509, KOREA

Bum C. Park
Eui S. Park

Samsung Electronics Co., Ltd.
#200 Myeongam-ri, Tangjeong-myeon
Asan-si, Chung-nam, 336-841, KOREA

ABSTRACT

In a typical FAB factory, various types of products are produced around the clock. Complex constraints and re-entrant flows make it difficult for a human scheduler to generate a production schedule based on his/her experience and knowledge. This paper introduces a simulation based FAB scheduler, SeePlan®, which was developed by the authors. A Korea based semi-conductor and LCD maker designated SeePlan as a standard advanced planning and scheduling solution and has used in several FAB factories around the world.

1 INTRODUCTION

High-Tech products including semiconductor chips, LCD (liquid crystal display) panels have been manufactured in FAB facilities. A FAB is highly capital-intensive requiring a few billion dollars of investment. Consequently, full-capacity production for high utilization and just-in-time production for on-time delivery with minimum WIP (work-in-process) are essential in FAB industry (Park et al. 2008).

In a typical FAB, a large number of product types are produced concurrently, 24 hours a day and 7 days a week. There exist various constrains and re-entrant flows which enable such expensive machines to be shared by all lots requiring the particular processing operation provided by the machine, even though they may be at different stages of their manufacturing cycle. For example, TFT (thin film transistor) needs 4 patterning cycles while 300 mm memory chip requires over 30 cycles which consist of deposition, photolithography, and etching processes. One TFT glass possibly becomes several different LC panels depending on the matched CF (color filter) glass. In a 7^{th} generation LCD FAB, eight LC cells of 40 inches panel size are graded or binned into 3~6 levels depending on their quality. Sometimes higher binned panels are downgraded to meet the due date of lower binned order. As a result, efficient planning and scheduling of FAB production is a big challenge.

Much research on dispatching rules and scheduling optimization for FAB has been conducted, and several commercial packages are reported and compete with each other. VMS Solutions, a spin-off venture from VMS (virtual manufacturing system) laboratory at KAIST (Korea advanced institute of science and technology) has been dedicated to develop information systems for various manufacturing industries including semi-conductor, LCD, automotive, and shipbuilding. The leading APS/SCM (advanced planning and scheduling/supply chain management) provider has developed a simulation based FAB scheduler, SeePlan®, which has over 10 reference sites including Samsung Electronics, Hyundai Motors, and Hankook Tire.

Core scheduling engine is explained in next section. SeePlan suites are described in Section 3, and case study implemented in a LCD maker is provided in Section 4. Conclusion is given in the final section.

2 FAB SCHEDULING ENGINE

Two approaches, optimization and simulation, are generally applied to the FAB scheduling. There are finite product batches and finite set of resource. Within a given time bucket, optimization approach finds an optimal solution which is a combination of resource and product. It is called as a *static combinatorial optimization approach*, and typically applies LP (linear programming) methods (Chung and Jang 2009). On the other hand, simulation approach defines decision variables called *handle* such as step target, equipment arrangement, dispatching rule. It finds an optimal solution continuously to change the decision variables according to the processing status and is called as a *dynamic optimal feedback control approach* as shown in Figure 1 (Choi and You 2006).

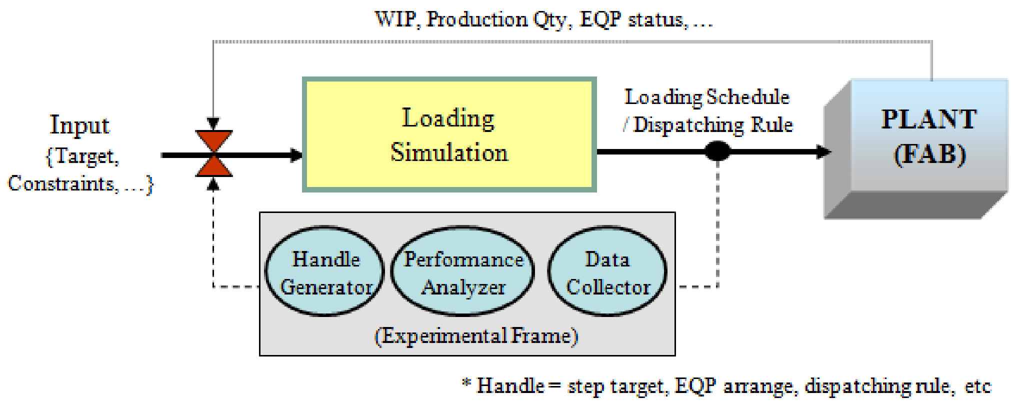


Figure 1: A dynamic optimal feedback control approach (Choi and You 2006)

SeePlan generates In/Out plans (production plan and release plan) from target production quantity and current WIP. The backward pegging engine determines the FAB-in profile from a given FAB out target taking into account the capacity of the FAB. The forward loading simulation engine generates loading schedule of each equipment in the Fab and production plan by a discrete event simulation with dispatching rules (Park et al. 2008).

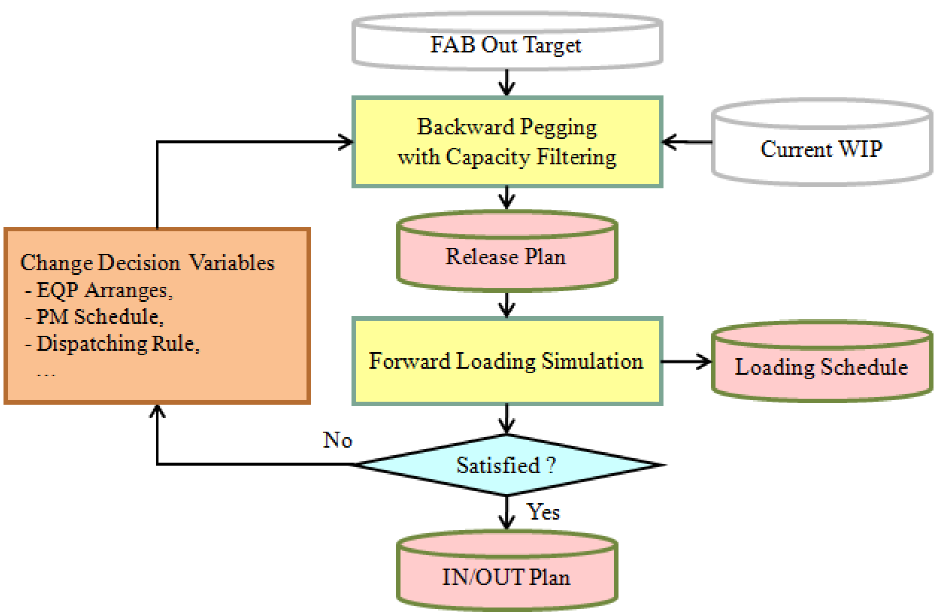


Figure 2: FAB scheduling procedure (Park et al. 2008)

2.1 Backward Pegging

This subsection focuses on a lot-order assignment problem called *pegging*. Pegging is a process of labeling WIP lots for a target order which is specified by the due date, quantity, and product specifications including customer information. It decides in/out target for each step, gives current WIP position for each demand, and calculates the latest possible start time (LPST) for each lot. As a result, we can get the release plan to meet the out target considering current WIP and machine status.

As shown in Figure 3, *out-target for step i* is converted to *in-target* as the following equations:

Due date: in-time = out-time – RUN-TAT (turn around time)

Quantity: in-qty = (out-qty – wip-qty) / step-yield

Out target for step *i-1* can be calculated with WAIT TAT and 100% of yield in the same manner. We finally get the in-target for the first step through the recursive calculation. Note that a target whose due date is earlier than simulation time means the demand is already late.

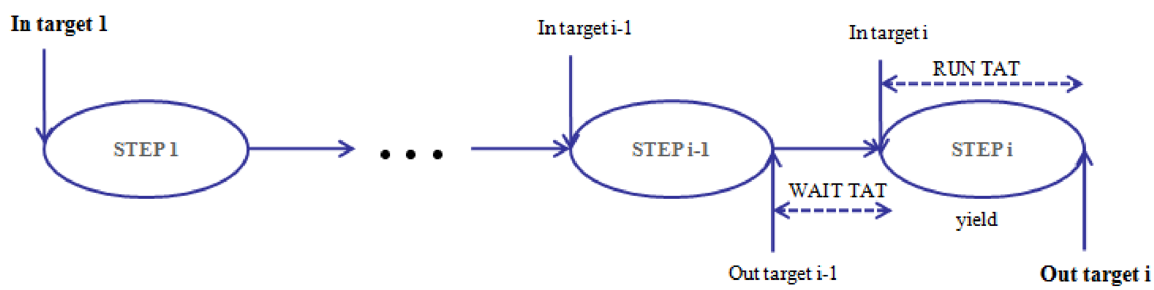


Figure 3: Calculation of In/Out target for each step

Depending on the business logic, we have to set the priority in selecting a target demand and a lot. We may select upper bin target first and patron customer's order next in target selection. We also apply a priority rule of minimal bin WIP first and bin-down next in WIP selection. As mentioned earlier, one type of wafer from the front-end possibly becomes tens of different semiconductor products depending on the attached material and the required specifications. Branch-off, binning, and substitution require a careful consideration (Chung and Jang 2009).

SeePlan supports three types of pegging methods, hard-peg, soft-peg, and mix-peg (See Wu 2003 for more details). According to the objective, various pegging algorithms including minimizing total tardiness of the orders (Kim et al. 2008) are provided. A *backward capacity filtering* (Choi and Seo 2008) which considers bottleneck resource such as photo-lithography is also compatible with SeePlan. Figure 4 shows capacity filtering concept. In the top graphs of the figure, the blue line represents initial capacity profile for a bottleneck equipment while green line shows out target profile. The portion of loading profile above the capacity is shifted to the previous time section shown in the bottom.

2.2 Forward Loading Simulation

Loading simulation concept came from the simple observation on the manufacturing process. When a job arrives, an idle machine loads and processes it. After completion, the machine unloads the job, and it moves to the next step. The loading simulation model focuses on the flow of *job* and loading/unloading behavior of *resource*. For simplicity, we may define two *events* by resources, LOADING and UNLOADING, and two *states* for jobs, RUN and WAIT. When a LOADING event occurs, the state of job is changed to RUN, and UNLOADING event is reserved to be invoked in a processing time for a next event. A discrete event simulation (DEVS) engine advances the time to generate next event. Dispatching rule helps the resource to select a proper job when a UNLOADING event occurs. As shown in Figure 5, the loading simulation engine generates loading schedule for each equipment in the FAB and lot history on the basis of three master data: bill of process (BOP) model, resource model, and dispatching rule. The current WIP is initialized at the beginning of simulation. Some are located in the buffer, and others in the middle of processing on a machine. Along with WIP, release plan is used as an input. It specifies product type, quantity, and release sequence for each equipment of the first step resource group. The simulation result can be analyzed to see key performance indices (KPI) including resource utilization, productivity, and WIP fluctuations.

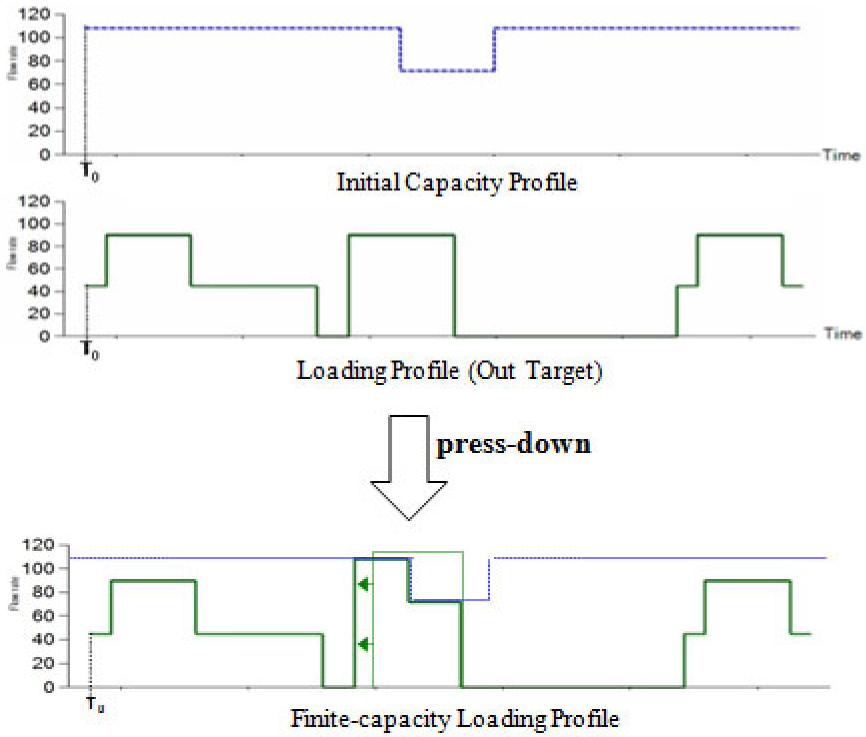


Figure 4: Backward capacity filtering concept (Choi and Seo 2008)

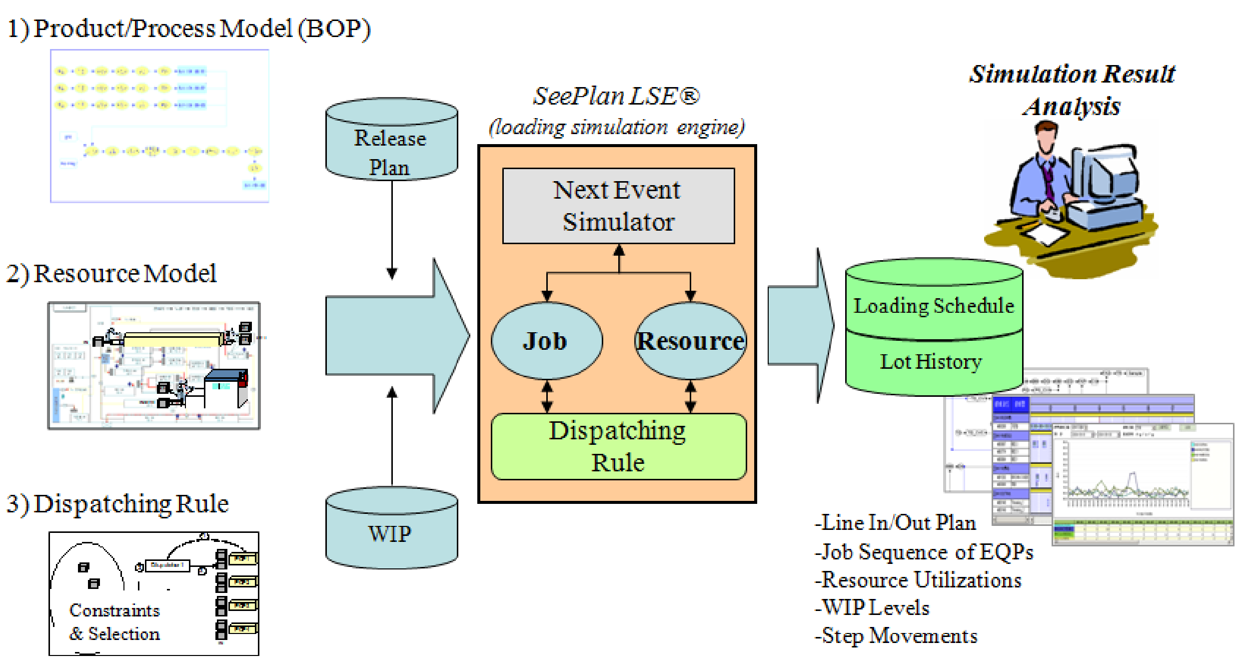


Figure 5: Overview of loading simulation implemented in SeePlan LSE®

BOP model is a network model which combines BOM (bill of material) and process routing. It consists of part(□), process(○) and transition(→) as shown in Figure 6. If processes are removed from BOP model, it turns to BOM tree. If parts are removed, it is similar to PERT (program evaluation and review technique) chart. BOP model contains step sequence, loadable resource list and tact/flow time for each step, and average transfer time.

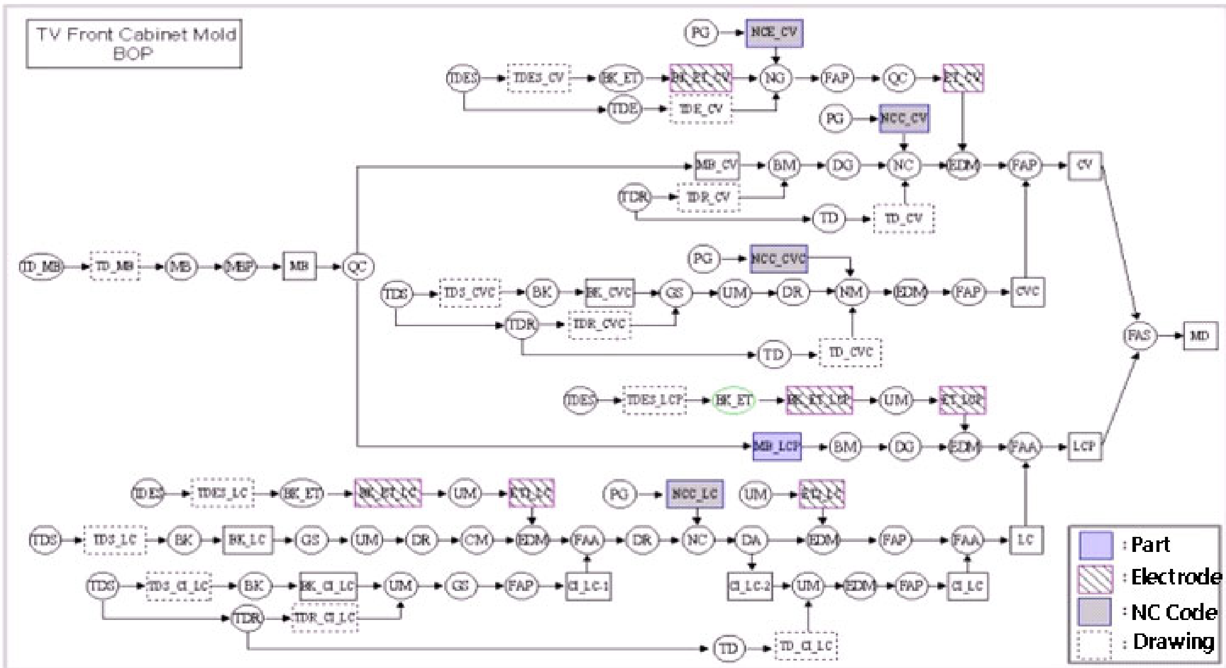
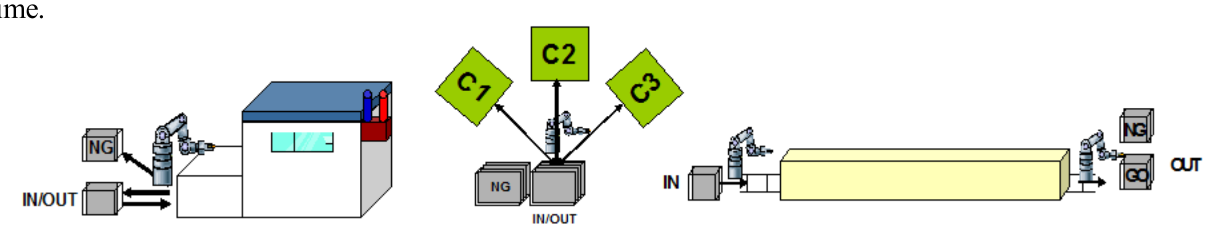


Figure 6: BOM model example

A resource is characterized by handling unit, processing type, and defect treatment policy. Handling unit could be different between loading and unloading even in the same facility. It can be a glass, a cassette which contains a set of glasses or cells, or a batch which is composed of several cassettes in LCD manufacturing. As shown in Figure 7, inline type has different in-port and out-port while table type and chamber type resource shares the same in/out port. Table type can load only one job while chamber and inline type can process multiple jobs at a time. Resource group indicates standard step to be processed, jig capacity, setup crew capacity, and list of unit resources. Each resource has dispatching rule and tact/flow time.



(a) Table Type (b) Chamber Type (c) Inline Type

Figure 7: Resource type

Dispatching rules are used to decide the priority for fulfilling orders. They control the flow of lots and decide production performance. Proper dispatching rules are selected to satisfy the objective such as due-date satisfaction, throughput maximization assuming machine idle avoidance, and WIP/TAT minimization. Typical examples include first-in-first-out (FIFO), earliest-due-date (EDD), and shortest processing time (SPT). Some objectives require a rule which looks ahead and behind for better performance. Usually multi-objectives are employed and conflict with each other. Gupta and Sivakumar (2002) proposed multi-objective scheduling optimization with scaling factor for each objective.

3 SEEPLAN SUITES

SeePlan suite includes SeePlan LSE®, SeePlan APS®, and SeePlan Studio® (VMS-Solutions 2010). *SeePlan LSE* which is the core part of SeePlan separates the simulation model with business logics from the simulation engine. Data model and business rules are defined in *Modeler* in Figure 8. As described in the previous section, *Simulator* conducts backward pegging and forward loading simulation with a simulation model predefined in *Modeler*.

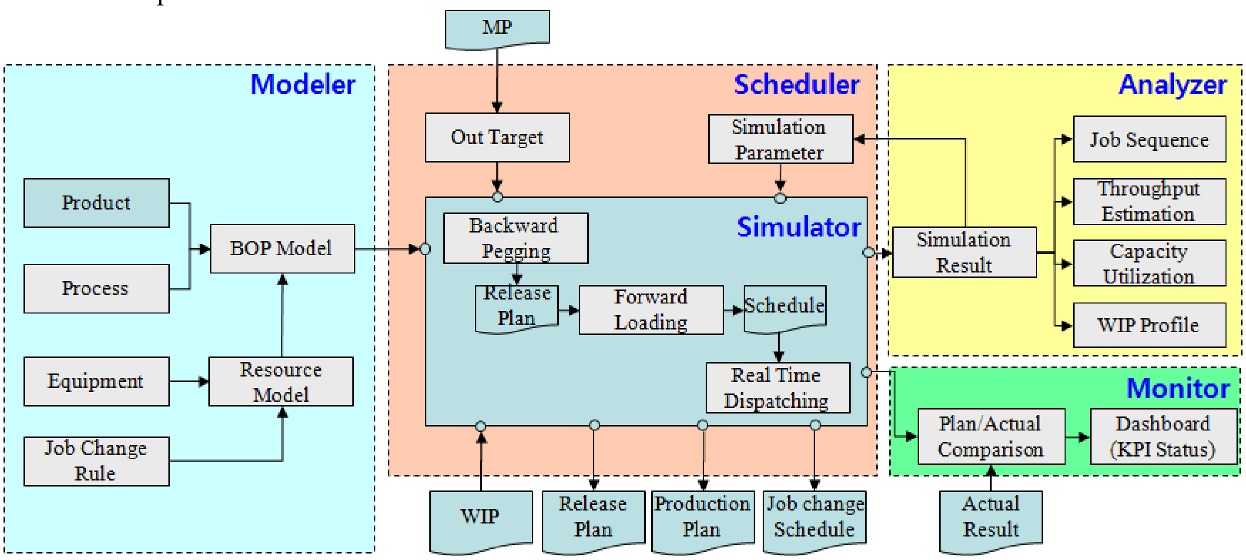


Figure 8: SeePlan system architecture

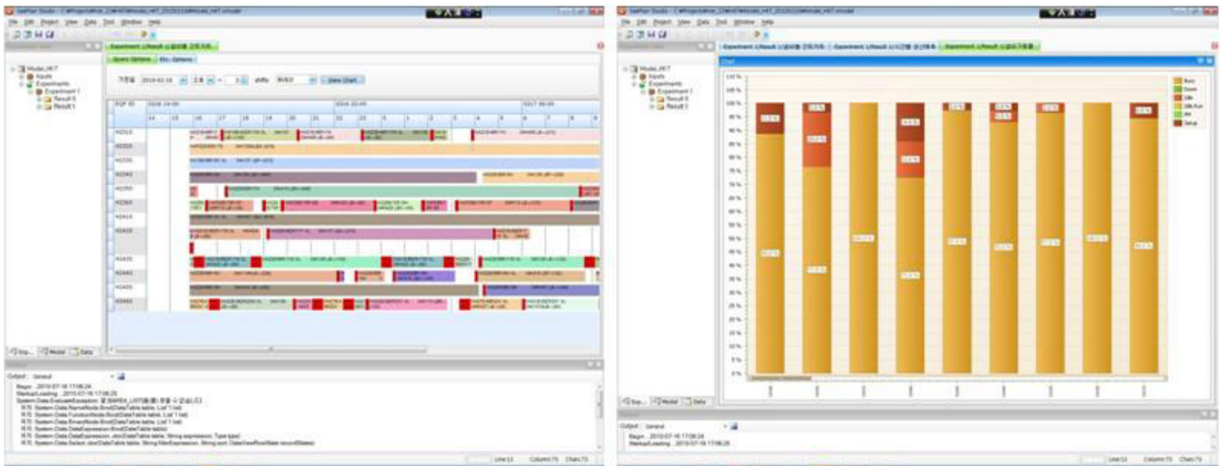
Shop floor managers or planners usually uses *SeePlan APS* which provides *Scheduler* and *Monitor* modules. Up-to-date MP (master plan) and WIP interfaced with enterprise data mart are given to *SeePlan APS*, which runs the simulation engine and generates release plan as well as production plan. *SeePlan APS* visualizes the resultant production progress and resource loading and compares with actual progress with Gantt chart. *Monitor* indicates KPI values including capacity utilization (Figure 9).

As a stand-alone simulator, *SeePlan Studio* reads the file to which *SeePlan APS* saved the simulation result. It enables the user to do what-if simulation by changing the simulation parameters, *i.e.* handles. *Analyzer* helps the user compare the results and make a good decision.

4 CASE STUDY

Figure 10 shows the overall business architecture of LCD module production management. When weekly MP is issued by the MPS (master planning system), the WPS (weekly planning system) performs finite capacity planning to generate a feasible daily production plan for the DPS (daily planning & scheduling) system which is implemented with *SeePlan APS*®. The DPS system generates detailed loading schedules for the FABs (TFT, CF, LC) and Module line (Park et al. 2008).

Since there are many LCD factories at Samsung, the MPS allocates customer demands to each factory in the form of weekly MP with a planning horizon of 13 weeks. The WPS receives weekly MP from the MPS once a week and performs finite capacity planning to generate 1) feasible daily production plans for two week periods, 2) purchase orders for the suppliers, 3) an MP progress report for the sales department, and 4) feedback information for the MPS regarding the feasibility of the weekly MP (the MP is adjusted if necessary, by the WPS).



(a) Gantt chart showing loading status (b) Bar chart indicating capacity utilization

Figure 9: Simulation result analysis in SeePlan Studio®

The DPS system converts the daily production plans into detailed 3-day loading schedules for each area (i.e., TFT FAB, CF FAB, LC FAB, and Module line), taking into account the WIP and equipment status (e.g., preventive maintenance schedule). It also generates 3-day delivery orders for the suppliers, 1-week shipping plans for the sales people, and daily in-out target values for each area. The RTS (real-time scheduling) system of each FAB (TFT, CF, LC) uses the FAB's loading schedule provided by the DPS system to generate job change schedules for bottle-neck equipment groups in the FAB every 5~10 minutes. The daily input target and output target are sent to the MES (manufacturing execution system) of each area to be used as their daily release plan and production plan, respectively.

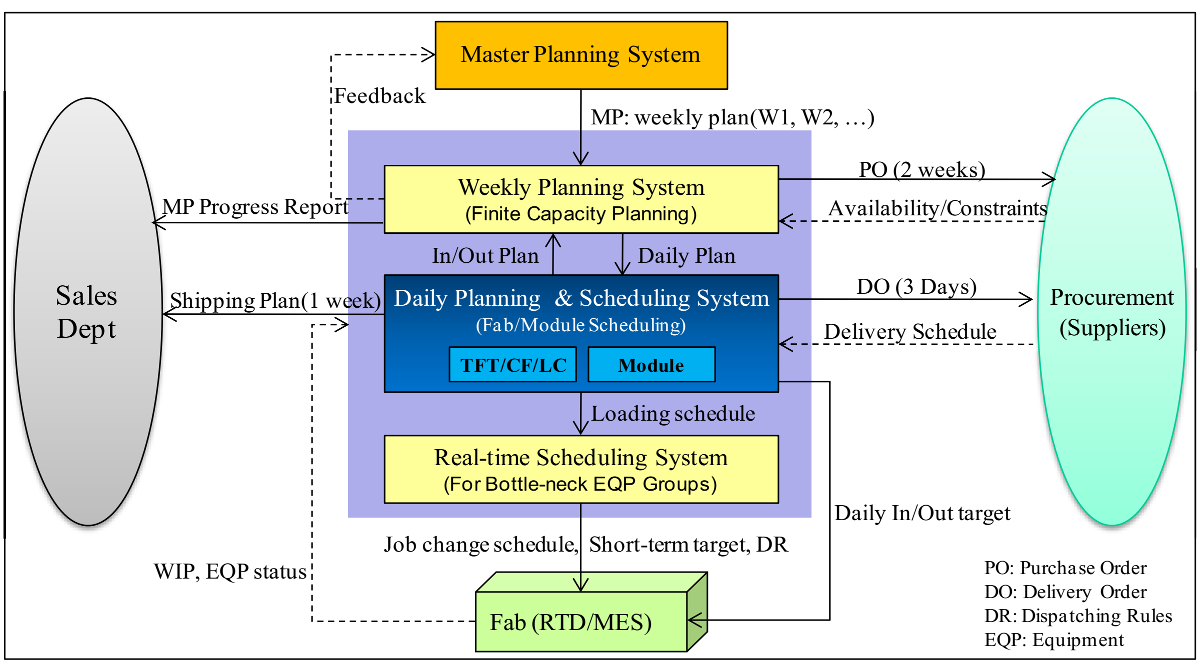


Figure 10: Business Architecture of LCD Production Management at a LCD Factory (Park et al. 2008)

The FAB-DPS system was installed at a large-size LCD Fab in 2006, and the system has been successfully used so far. During the time, the ratio of on-time delivery of LCD panels to the module line has increased to 92% (from 75%) and the turn-around time of LCD panel fabrication has been reduced by 35%. The Module-DPS system is also being used together with the weekly planning system. It has played a key role in supply chain management and has been expanding to other lines.

5 CONCLUSION

High-Tech products such as LCD, semi-conductor are produced through complex processes which consist of various manufacturing steps. It is difficult to obtain an optimal production schedule which takes into account various factors including equipment, WIP status, product mix and priority. Unexpected problems such as equipment break-down, material shortage make it difficult to follow the schedule which was created by a planner in the beginning of the term. SeePlan, an advanced planning and scheduling system (APS), generates a reliable schedule based on the current status and provides an easy function to reflect the abnormal changes flexibly.

ACKNOWLEDGMENTS

This research was conducted as a part of project for the Development of digital based real-time adaptive manufacturing system platform (Development of generation & verification technology for manufacturing control program) sponsored by Korea Ministry of Knowledge Economy.

REFERENCES

Choi, B.K., and N.K. You. 2006. Dispatching rules for dynamic scheduling of one-of-a-kind production. *International Journal of Computer Integrated Manufacturing* 19:383-392.

Choi, B.K., and J.C. Seo. 2008. Capacity-filtering algorithm for finite capacity planning of a flexible flow line. *International Journal of Production Research* 47:3363-3386.

Chung, J., and J. Jang. 2009. A WIP balancing procedure for throughput maximization in semiconductor fabrication. *IEEE Transactions on Semiconductor Manufacturing* 22:381-390.

Gupta, A.K., and A.I. Sivakumar. 2002. Simulation based multiobjective schedule optimization in semiconductor manufacturing. In *Proceedings of the 2002 Winter Simulation Conference* ed. E. Yücesan, C.H. Chen, J.L. Snowdon, and J.M. Charnes, 1862-1870. Piscataway, New Jersey: Institute of Electrical and Electronics Engineers, Inc.

Kim, Y.D., J.Y. Bang, K.Y. An, and S.K. Lim. 2008. A due-date-based algorithm for lot-order assignment in a semiconductor wafer fabrication facility. *IEEE Transactions on Semiconductor Manufacturing* 21:209-216.

Park, B.C., E.S. Park, B.K. Choi, B.H. Kim, and J.H. Lee. 2008. Simulation based planning and scheduling system for TFT-LCD FAB. In *Proceedings of the 2008 Winter Simulation Conference*, ed. S.J. Mason, R.R. Hill, L. Monch, O. Rose, T. Jefferson, and J.W. Fowler, 2271–2276. Piscataway, New Jersey: Institute of Electrical and Electronics Engineers, Inc.

VMS-Solutions. 2010. *SeePlan® Brochure*. Available via <http://www.vms-solutions.com/vms/downbox/seeplan.pdf> [accessed July 15, 2010].

Wu, T. W. 2003. Modular demand and supply pegging mechanism for semiconductor foundry. In *Proceedings of IEEE International Symposium on Semiconductor Manufacturing,* 325-328.

AUTHOR BIOGRAPHIES

KEYHOON KO is an executive director of VMS Solutions Co., Ltd. since 2003. He received a BS from Sungkyunkwan University in 1995, a MS from KAIST in 1997, and a Ph.D. from KAIST in 2003, all in Industrial Engineering. His main research interests are CAD/CAM, product lifecycle management, supply chain management, and simulation-based planning and scheduling. His email address is <fish@vms-solutions.com>.

SEOCK K. YOO is an executive director of VMS Solutions Co., Ltd. since 2005. He received a BS from Seoul National University in 1990, a MS from KAIST in 1999, and a Ph.D. from KAIST in 2005, all in Industrial Engineering. His research interest is simulation-based scheduling. His email address is <skyoo@vms-solutions.com>.

BYUNG H. KIM is the president of VMS Solutions Co., Ltd. since 2000. He received a BS from Sungkyunkwan University in 1993, a MS from KAIST in 1995, and a Ph.D. from KAIST in 2001, all in Industrial Engineering. His main interests are simulation-based scheduling and planning, manufacturing information systems, BPMS, and virtual manufacturing. His email address is <kbhee@vms-solutions.com>.

BUM C. PARK is a senior engineer of Samsung Electronics Co., Ltd. since 2004. He received a BS from Sungkyunkwan University in 1996, a MS from KAIST in 1998, and a Ph.D. from KAIST in 2004, all in Industrial Engineering. His main interests are simulation-based scheduling and planning, supply chain management, and real time dispatching. His email address is <bum-chul1004.park@samsung.com>.

EUI S. PARK is a vice president of Samsung Electronics Co., Ltd. He received a BS in Mechanical Engineering from Yonsei University in 1985, and a MS in Mechanical Engineering from KAIST in 1988 and a MS and Ph.D. in Electrical Engineering from the University of Michigan in 1998 and 1999, respectively. His main interests are scheduling & planning, production optimization, and material flow simulation. His email address is <euisu.park@samsung.com>.