

SIMULATION BASED PLANNING AND SCHEDULING SYSTEM FOR TFT-LCD FAB

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ABSTRACT

In a typical LCD factory, a large number of product types are produced concurrently, 24 hours a day and 365 days a year, and there exist various constraints and re-entrant flows in the manufacturing processes. As a result, efficient planning and scheduling of LCD production is a big challenge. Presented in this paper is a simulation-based DPS (daily planning & scheduling) system that was developed by the authors and is being used in a modern LCD Fab in Korea. Also presented in the paper are a business architecture of LCD production management, internal structure of the DPS system, and Fab scheduling logic. The DPS system was installed at a large-size LCD Fab in 2006, and the system has been successfully used for two years leading to a considerable increase in on-time production of LCD panels and a sharp decrease in turn-around time.

1 INTRODUCTION AND LITERATURE REVIEW

The LCD industry is growing fast as LCD monitors are increasingly used in TV sets and computers replacing CRT monitors. LCD modules are *made to order*, namely, an LCD factory is an MTO production system. New types of LCD modules are introduced continuously, and their life cycles are becoming shorter. A modern LCD factory is highly *capital-intensive* requiring a few billion dollars of investment. Thus, in order to be competitive in the global market, full-capacity production (for high utilization of Fab) and just-in-time production (for on-time delivery with minimum WIP) are essential in LCD manufacturing.

In a typical LCD factory, a large number of product types are produced concurrently, 24 hours a day and 365 days a year, and there exist various constraints and re-entrant flows in the manufacturing processes. As a result, efficient planning and scheduling of LCD production is a big challenge. Presented in this paper is a simulation-based DPS (daily planning & scheduling) system that was developed by the authors and is being used in modern LCD factories at Samsung Electronics Co. in Korea.

The existing studies on planning and scheduling of LCD production are rather limited in scope, focusing mainly on Module line. Jeong, Kim, and Lee (2001) proposed an LP (linear programming) based mathematical model for equipment assignments in Module line. They also proposed an LP model and a heuristic method for minimizing flow time while meeting customer demands (Jeong et al. 2002). Na et al. (2002) proposed a backward method of LCD production planning starting from a given delivery plan. Shin et al. (2004) proposed a heuristic algorithm to minimize tardiness and set-up changes in Module line operations. Lin et al. (2004) proposed a 'hierarchy planning model' for LCD production chain by combining a push-system concept with a pull-system concept. Subsequently, they proposed a 'hierarchical, combined push-pull, modular' approach to planning and scheduling of LCD production (Lin et al. 2006).

Presented in this paper is a simulation-based Fab scheduling system, called DPS system, that is being used at an LCD module maker in Korea. An overview of LCD manufacturing process is given in the next section, and a business architecture of LCD production management is presented in Section 3. Major functions of a Fab-DPS sys-

tem are described in Section 4, and a brief description of Fab scheduling logic is given in Section 5. Conclusions and discussions are given in the final section.

2 OVERVIEW OF LCD MANUFACTURING PROCESS

A TFT-LCD (thin-film transistor liquid crystal display) module, or *LCD module* for short, consists of an LCD cell, BLU (back light unit), PCB, driving IC chips, and plastic frames. An *LCD cell*, which is the key component of an LCD module, consists of a TFT glass, a CF (color filter) glass, and LC (liquid crystal) filled in between the TFT glass and CF glass. Thus, as shown in Figure 1, an LCD factory is composed of 1) a *TFT Fab* where thin film transistors are formed on raw glasses, 2) a *CF Fab* where color filters are formed on raw glasses, 3) an *LC Fab* where TFT and CF glasses are assembled and liquid crystal is filled in between, and cut into *panel-sizes*, and 4) a *Module line* where final assembly operations are performed mostly by human operators.

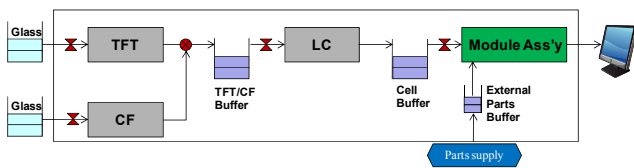


Figure 1: Overview of LCD manufacturing process

The fabrication process of TFT is similar to that of semiconductor wafer (Lin et al. 2004): It basically is a series of layer *patterning* operations. There are four or five layers in a TFT depending on product type. The patterning operations of a five-layer TFT are 1) gate layer patterning, 2) active area layer patterning, 3) source/drain layer patterning, 4) passivation layer patterning, and 5) IZO layer patterning. Each layer patterning operation consists of cleaning, deposition, photo-lithography (photo-resist coat-

ing, exposure, and development), etching, stripping, and inspection *steps*. Fabrication of a typical TFT requires 30~40 steps and its *turn-around time* is about 48 hours. The CF fabrication process is similar to the TFT fabrication process. It requires four or five layer-patterning operations, consisting of 15~20 steps, with a Fab turn-around time of about 24 hours. Both TFT Fab and CF Fab are essentially a job shop having re-entrant flows. Usually, photo-lithography machines, which are more expensive than other equipments, are bottle-neck equipments.

The LC Fab produces LCD cells from TFT glasses and CF glasses, with a turn-around time of 10~12 hours, by employing about 15 steps. In a 7th generation LCD Fab, for example, eight LCD cells of 40 inches panel size are produced from a pair of TFT and CF glasses. The produced LCD cells are graded into 3~6 levels depending on their quality level. In the Module line, an LCD cell is assembled with *external parts* such as BLU, polarizer, and PCB. For a given *product type* of LCD cell, 10~30 *options* of LCD module are obtained depending on the specifications of the external parts. Since there are more than a dozen product (LCD cell) types, the total number of options (of LCD module) is quite large. Thus, careful synchronization of external parts supply with internal production schedule of LCD cells is very critical.

3 BUSINESS ARCHITECTURE OF LCD PRODUCTION MANAGEMENT

Shown in Figure 2 is the overall business architecture of LCD module production management. When weekly MP (master plan) is issued by the master planning system, the weekly planning system performs finite capacity planning to generate a feasible daily production plan for the DPS (daily planning & scheduling) system. The DPS system generates detailed loading schedules for the Fabs (TFT, CF, LC) and Module line.

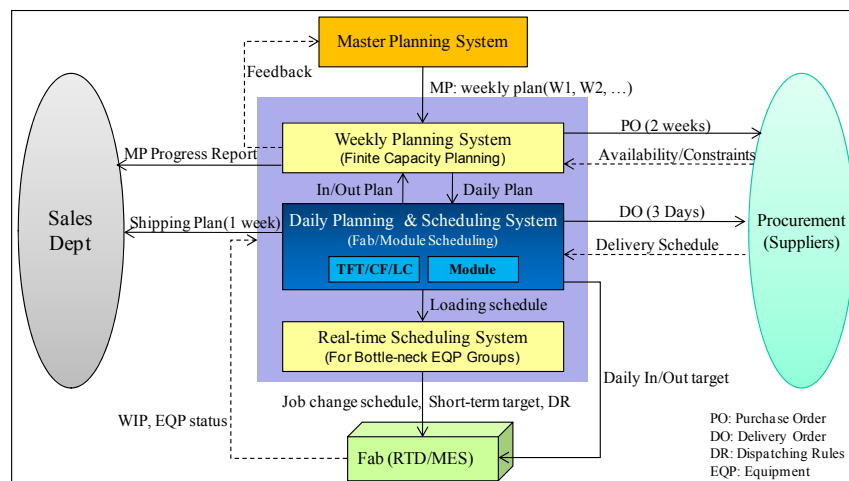


Figure 2: Business Architecture of LCD Production Management at a LCD Factory

Since there are many LCD factories at Samsung, the master planning system (MPS) allocates customer demands to each factory in the form of *weekly MP* with a planning horizon of 13 weeks. The weekly planning system (WPS) receives weekly MP from the MPS once a week and performs finite capacity planning to generate 1) feasible *daily production plans* for two week periods, 2) *purchase orders* for the suppliers, 3) an *MP progress report* for the sales department, and 4) feedback information for the MPS regarding the feasibility of the weekly MP (the MP is adjusted if necessary, by the WPS).

The DPS system converts the daily production plans into detailed 3-day *loading schedules* for each area (i.e., TFT Fab, CF Fab, LC Fab, and Module line), taking into account the WIP and equipment status (e.g., preventive maintenance schedule). It also generates 3-day *delivery orders* for the suppliers, 1-week *shipping plans* for the sales people, and *daily in-out target* values for each area. The real-time scheduling (RTS) system of each Fab (TFT, CF, LC) uses the Fab's *loading schedule* provided by the DPS system to generate *job change schedules* for bottle-neck equipment groups in the Fab every 5~10 minutes. The *daily input target* and *output target* are sent to the MES (manufacturing execution system) of each area to be used as their *daily release plan* and *production plan*, respectively.

4 FUNCTIONS OF DAILY PLANNING AND SCHEDULING SYSTEM

In this section, the internal structure of the daily planning and scheduling (DPS) system is described in more detail. The DPS system is divided into a *Fab-DPS system* covering the three Fabs (TFT, CF and LC) and a *Module-DPS system* for the Module line. The Module-DPS system receives daily production target of the Module line from the weekly planning system (WPS) and generates daily *LC-Out target* (daily production requirements of the LC Fab). Using the LC-Out target as input, the Fab-DPS system generates per-shift *In Plan* (release plan) and *Out Plan* (production plan) of the TFT, CF, and LC Fabs which are fed back to the Module-DPS system as depicted in Figure 3. Then, with this feedback information, the Module-DPS system generates 1) the *release plan and production plan* of the Module line, 2) *delivery orders* for the suppliers, and 3) *shipping plan* for the sales department.

The core part of the Fab-DPS system is the *Fab scheduling engine* that performs capacity filtering and loading simulation operations and generates In/Out Plans and Loading Schedules of the Fabs (TFT/CF/LC). More details about the Fab scheduling engine will be given in the next section. Also included in the Fab-DPS system are additional software modules such as Master data manager, Progress monitor, Bottleneck EQP planner, Release order planner, KPI analyzer, and Decision variable editor.

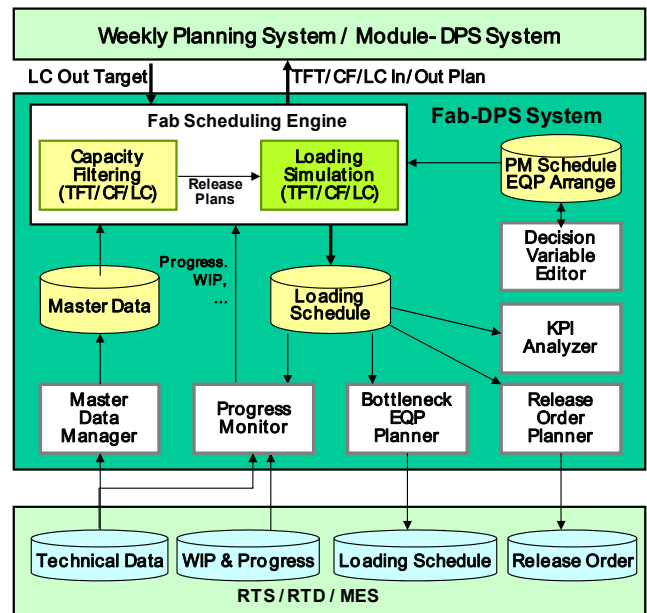


Figure 3: DPS System Architecture

Master Data Manager is responsible for maintaining correct master data which is one of the essential (and difficult) tasks in the Fab-DPS system. Master data in the Fab-DPS system includes:

- BOM and routing data for each product type,
- Flow time, tact time, and yield data for each processing step
- Simulation model type, setup time, dispatching rule, and down-time data for each equipment
- Loadable relationship between steps and equipments and EQP-arrange data
- Photo mask and inspection probe data

Master Data Manager periodically updates the master data DB by retrieving information from the technical data DB that is supported by the MES system in the Fabs.

Progress Monitor receives various shop-floor status data and work progress data from the MES system and compares the actual progresses against the planned targets in the loading schedule DB. If any abnormal delay is observed it issues relevant warning messages to respective supervisors. *Bottleneck EQP Planner* triggers the execution of loading simulation every 1~2 hours to obtain detailed *loading schedules* of bottleneck equipments (photolithography equipments in TFT/CF Fabs and visual inspection equipments in LC Fab) and sends the results to respective RTS systems in the Fabs. *Release Order Planner* retrieves the *firm release plans* of the Fabs and sends *release orders* to respective MES systems.

KPI Analyzer makes periodic analyses of *key performance indexes* such as equipment utilization (percentages of busy, idle, setup and PM), equipment productivity (ratio of actual production and target production per period), WIP

fluctuation, and input (released volume) and output (produced volume) of each Fab. Based on the observed KPI values, *decision variables* may be adjusted by using *Decision Variable Editor*. Major decision variables for Fab scheduling are PM (preventive maintenance) schedule, EQP arrange (pre-assignment of EQP to processing steps), dispatching rule, size and timing of batch release, and product priority. The Fab-DPS system is executed again with the adjusted decision variables. This analysis-adjustment process may be repeated several times until a satisfactory result is obtained.

The DPS system was implemented with C# language under the .NET environment, and all the UIs (user interfaces) are Web-based, developed by using ASP.NET. Shown in Figure 4 is an example of decision variable adjustment (a UI for adjusting EQP Arrange). Figure 5 shows a Gantt chart representation of loading schedules for a group of bottleneck equipments (photo-lithography equipments).

| Layer | Seq STEP | M/C | Matching EQP | EQP Model | TP101 | TP102 | TP103 | TP201 | TP202 |
|---------|-------------------|--------|--------------|-----------|-------|-------|-------|-------|-------|
| T_1_VR1 | T110XT_1ST_CLN) | TCLM01 | Inline | | 60 | 60 | 60 | 60 | 60 |
| | | TCLM02 | Inline | | 60 | 60 | 60 | 60 | 60 |
| | T120XT_1ST_DEFO) | TDEP01 | Inline | | 66 | 66 | 66 | 66 | 66 |
| | | TDEP02 | Inline | | 66 | 66 | 66 | 66 | 66 |
| | T130XT_1ST_PHOTO) | TPH01 | Inline | | 96 | 96 | 96 | 96 | 96 |
| | | TPH02 | Inline | | 96 | 96 | 96 | 96 | 96 |
| T_1_VR2 | T210XT_2ND_CLN) | TCLM03 | Inline | | 60 | 60 | 60 | 60 | 60 |
| | | TCLM04 | Inline | | 60 | 60 | 60 | 60 | 60 |
| | T220XT_2ND_DEFO) | TDEP03 | Inline | | 90 | 90 | 90 | 90 | 90 |
| | | TDEP04 | Inline | | 90 | 90 | 90 | 90 | 90 |
| | T230XT_2ND_PHOTO) | TPH03 | Inline | | 90 | 90 | 90 | 90 | 90 |
| | | TPH04 | Inline | | 90 | 90 | 90 | 90 | 90 |
| T_1_VR3 | T310XT_3RD_CLN) | TCLM05 | Inline | | 60 | 60 | 60 | 60 | 60 |
| | | TCLM06 | Inline | | 60 | 60 | 60 | 60 | 60 |
| | T320XT_3RD_DEFO) | TDEP05 | Inline | | 72 | 72 | 72 | 72 | 72 |
| | | TDEP06 | Inline | | 72 | 72 | 72 | 72 | 72 |
| | | TDEP07 | Inline | | 72 | 72 | 72 | 72 | 72 |
| | | TDEP08 | Inline | | 72 | 72 | 72 | 72 | 72 |

Figure 4: Decision Variable Editing (Equipment Arrange)

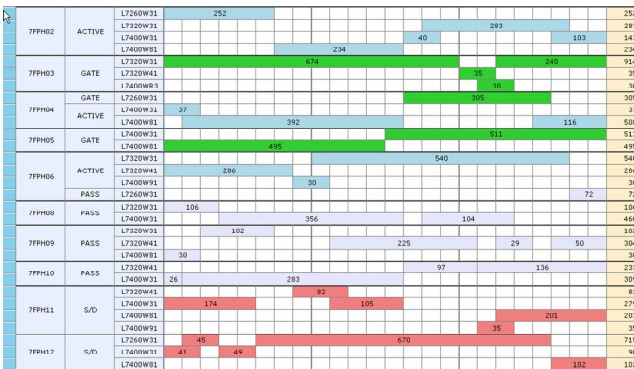


Figure 5: Loading Schedule of Bottleneck Equipments

5 FAB SCHEDULING LOGIC

This section briefly describes how Fab scheduling is carried out by the Fab scheduling engine of the Fab-DPS system. The overall *Fab scheduling logic* is given in Figure 6 and it consists of three phases: Capacity filtering, TFT/CF Fab loading simulation, and LC Fab loading simulation.

The backward capacity filtering algorithm(Choi and Seo 2008) determines the Fab-in profile (i.e., a sequence of the segments specified by load-rate, loading quantity, start time, end time and job type) of a Fab from a given production plan taking into account the capacity of the Fab. The loading simulation method(Kim 2001) generates the loading schedule of each equipment in the Fab and production plan by a discrete event simulation from a given release plan and dispatching rules. Input data for the Fab scheduling engine are per-shift *LC-out targets* for one week periods and the current WIP of the TFT/CF/LC Fabs, and its outputs are TFT/CF Fab loading schedules, LC Fab loading schedules, and TFT/CF/LC In/Out plans.

In the capacity filtering phase, 1) *backward capacity filtering* operations (Choi and Seo 2008) are performed for the LC Fab using the *LC-out targets* (i.e., per-shift LC production requirements), taking into account the current WIP in the Fab, to obtain the *Fab-in profile* of LC Fab, 2) the LC Fab-in profile is converted to *Fab-out profiles* of TFT/CF Fabs, 3) backward capacity filtering operations are performed for the TFT/CF Fabs using their Fab-out profiles to obtain TFT/CF Fab-in profiles, and finally 4) *TFT-in plan* and *CF-in plan* (i.e., *release plans*) are obtained from their Fab-in profiles. During the *release planning*, a number of constraints have to be taken into account. Examples of constraints are 1) the current batches being released should not be split, 2) user-designated batches must be released at their pre-determined release times, 3) batch sizes must be within their pre-defined limits, and 4) the batch release sequence of the CF Fab must be in sync with that of the TFT Fab.

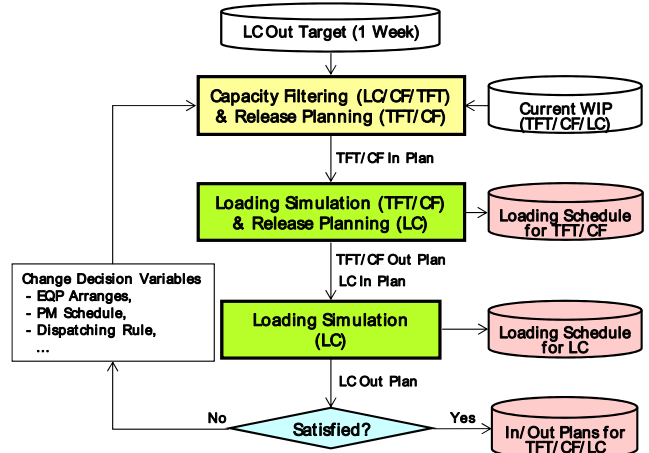


Figure 6: Fab Scheduling Procedure

During the second phase of Fab scheduling, 1) *loading simulation* (Kim 2001) is performed for the TFT Fab using the *TFT-in plan* (i.e., release plan) to obtain *TFT-out plan* and detailed loading schedules of TFT Fab, 2) another loading simulation is performed for the CF Fab, and 3) *release planning* is performed for the LC Fab to obtain LC-in

plan. A proprietary package (VMS Solutions 2006) is used for the loading simulation. Notice that we use the term “In plan” and “Out plan” as shortened expressions for ‘release plan’ and ‘production plan’, respectively. During the third phase of Fab scheduling, loading simulation is performed for the LC Fab using the LC-in plan to obtain LC-out plan. If the obtained LC-out plan satisfies the LC-out target, the Fab scheduling is completed. Otherwise, decision variables (e.g., EQP arrange, PM schedule, dispatching rules) are adjusted, and the Fab scheduling cycle is repeated.

6 CONCLUSION AND DISCUSSIONS

In this paper, we presented a simulation-based DPS (daily planning & scheduling) system for LCD production management. The DPS system is composed of a Fab-DPS system covering TFT/CF/LC Fabs and a Module-DPS system for Module line. The Fab-DPS system was installed at a large-size LCD Fab in 2006, and the system has been successfully used for two years. During the two-year period, the ratio of on-time delivery of LCD panels to the module line has increased to 92% (from 75%) and the turn-around time of LCD panel fabrication has been reduced by 35%. The Module-DPS system is also being used together with the weekly planning system.

Simulation-based Fab scheduling made it easier to anticipate future schedule changes (by simulating various ‘what-if’ scenarios based on real-time shop-floor data), and as a result, production discrepancies could be reduced considerably (by quickly responding to changes in fabrication lines). The DPS system promoted sharing of production plans and actual progress data among the various people involved in production management, leading to a shortened decision-making cycle with reduced communication errors.

However, it is quite ‘resource-intensive’ to maintain valid master data and to acquire real-time progress data from the Fabs. Another difficulty with the simulation-based Fab scheduling is finding (or defining) proper ‘handles’ for adjusting the decision variables (refer to Figure 6). In particular, finding ‘optimal’ dispatching rules is a big challenge deserving further research.

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