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SIMULATION ANALYSIS OF SEMICONDUCTOR MANUFACTURING WITH SMALL LOT SIZE AND BATCH TOOL REPLACEMENTS

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ABSTRACT

Long cycle times in semiconductor manufacuring represent an increasing challenge for the industry and lead to a growing need of break-through approaches to reduce it. Small lot sizes and the conversion of batch processes to mini-batch or single-wafer processes are widely regarded as a promising means for a step-wise cycle time reduction. However, there is still a lack of comprehensive and meaningful studies. In this paper we present first results of our modeling and simulation assessment. Our simulation analysis shows that small lot size and the replacement of batch tools with mini-batch or single wafer tools are beneficial but lot size reduction lacks persuasive effectiveness if reduced by more than half.

1 INTRODUCTION

Time is one of the critical success factors for competitive manufacturing in general. Having very unique characteristics, the semiconductor industry was not captured by this strategic focus to the same extent as many other industries. However, recent market and product dynamics make the need for advancement more imminent (Liu 2005). Therefore approaches to achieve a step-wise reduction in cycle time are needed in semiconductor manufacturing.

Small lot size and single wafer tools have been identified by several IC manufacturers as a potential production system shift to drive down cycle time (e.g. (Grose 2007, Greenberg 2007)). Limited simulation work on this change has been done by Wakabayashi et al. (Wakabayashi et al. 2004) for small lot size and by Koshti and Ward (Koshti and Ward 2008) for ultra-small lot size, but a solid analysis on the expected cycle time reduction is still missing.

We established a basis in previous publications. In (Schmidt and Rose 2007a) we gave an overview of possible production system changes enabling shorter cycle time and set references for the corresponding raw process time reduction. In (Schmidt and Rose 2007b) we analyzed how queueing time changes for a single operation with lot size reduction. Additionally, we presented ideas how to overcome challenges of the small lot size approach in (Zimmerhackl et al. 2007), (Schmidt and Rose 2007a), and, (Schmidt and Rose 2008).

This paper is organized as follows. In Section 2 we present the fab simulation model used in our analysis with product, toolset and flow characteristics. We introduce the set of cycle time components in Section 3, which we use to facilitate the analysis and show dependancies. Section 4 and 5 give a summary of the fab simulation results obtained for lot size reduction and different toolsets including batch tools in the baseline version, as well as mini-batch and single wafer tool replacements in another scenario. We devote Section 6 to considerations and simulation experiments regarding the influence of setup times on cycle time performance of reduced lot size and Section 7 concludes the paper with a short summary.

2 FAB SIMULATION MODEL

We created a simulation model that is representative for a typical 300mm semiconductor manufacturing environment. The following list gives an overview of the simulation model's main characteristics in its baseline version.

- Fab profile:
  - Products: one product.
  - Flow complexity: 23 mask layers; 7 metal layers.
  - Max. static capacity: 960 waferstarts/day (40 lotstarts per day at 24 wafer lot size).
- Flow:
  - 209 process steps.
  - 165 metrology and 4 test steps.
- Tools:
  - 38 process workstations, 175 tools.

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  - 9 metrology workstations, 106 tools.
  - 2 test workstations, 40 tools.
- Availability:
  - failures: MTTR & MTBF.
  - maintenance: up to 6 types of preventive maintenance (daily to bi-yearly).
  - all downtimes modelled as non-preemptive.
- Process times: Per wafer or per batch time and per lot delay.
- Dispatching:
  - Batching context: 18 batching contexts at 9 batch workstations with 80 operations.
  - Batching rule: Wait for full batch.
  - Dispatching: FIFO with setup avoidance.
- Transport: Static 0.15 h delay per operation.

Some points in this list require additional discussion. In its baseline configuration the model includes only one product in order to exclude disturbances caused by product variety. Additionally we have kept the size of the fab at a small to medium level with respect to flow complexity and wafer starts. This holds the simulation run time of scenarios with smaller lot sizes at an acceptable level.

Another specification might sound a little odd at first. Although current standard lot size is 25 wafers, we have chosen a lot size of 24 wafers as our baseline. Yet, this change enables a constant batch loading for the lot sizes under consideration 24, 12, 6, and, 2 wafers. Otherwise we could not distinguish the effects of lot size reduction and batch loading changes. Only the baseline of 24 wafers produces pure results for the lot size reduction.

Our static transport delay looks weird at first glance. It is unrealistic to expect that current material handling systems are able to support reduced lot size with the same performance because lot size reduction goes hand in hand with transport volume increase. However, looking at this issue from another side, the need for fast on time delivery increases with lot size reduction and how should that be accomplished if transport times increase? Therefore we have chosen to assume that transport time stays the same for all lot size scenarios keeping in mind that the material handling system might need significant redesign to achieve this. Additionally, we assume that material handling challenges like reduced carrier exchange times are solved, e.g., as we showed in (Zimmerhackl et al. 2007), and do not impact equipment productivity.

Two important characteristics are missing in the list: Setups and Measurements. We have included setup times in the baseline model only where it is definitely unavoidable: At implant operations. For other potential setups, we created separate scenarios which we discuss in Section 6. Our metrology modeling is subject of the next two paragraphs.

It is unclear how sampling needs to change with lot size reduction. For some applications representing simple process monitoring, the sampling which requires a measurement after a fixed number of wafers is unlikely to change. Other applications might at least depend on sophisticated scheduling efforts to avoid increasing the number of necessary measurements. However, metrology cycle time decreases very significantly with lot size as will be apparent in Section 4.1. Therefore, the necessity to assess the question of a possible small increase in measurements in great detail does not arise.

In our simulation model we took a general approach with combined skip rate increase and wafer sampling reduction assuming that the total measurement time stays the same. This might, e.g., mean that the number of wafers that are actually measured stays the same, although this is not necessarily a consequence of the sampling setup used. Table 1 specifies the sampling characteristics used in the simulation for all metrology operations independently of its application.

Table 1: Sampling at different lot sizes under consideration.

Lot size	Lot skip rate	Relative lot processing time
24	70%	1
12	77.5%	0.67
6	85%	0.5
2	92.5%	0.33

The verification of the simulation model was done in two steps. First all results that are not subject to variation are checked against pre-determined values, as e.g. precalculated utilizations based on toolcount and availability in Figure 1. Then plausibility checks were performed to assess whether results influenced by randomness (queueing time) are reasonable compared to single operation assessments performed with queueing models and single operation simulation in (Schmidt and Rose 2007b).

We conduct our simulation experiments with Factory Explorer from WWK. In all experiments we vary the fab loading between 50% and 97.5% in 2.5% increments, however, we show most results only for an exemplary 92.5% loading representing an almost fully loaded fab. At each loading we run the simulation for 51 years including a 1 year warm-up period.

3 CYCLE TIME COMPONENTS

The cycle time that lots spend while passing the complete process flow is divided into queue time and process time (see Figure 2). For a better assessment of the effects we classify these into smaller cycle time components having

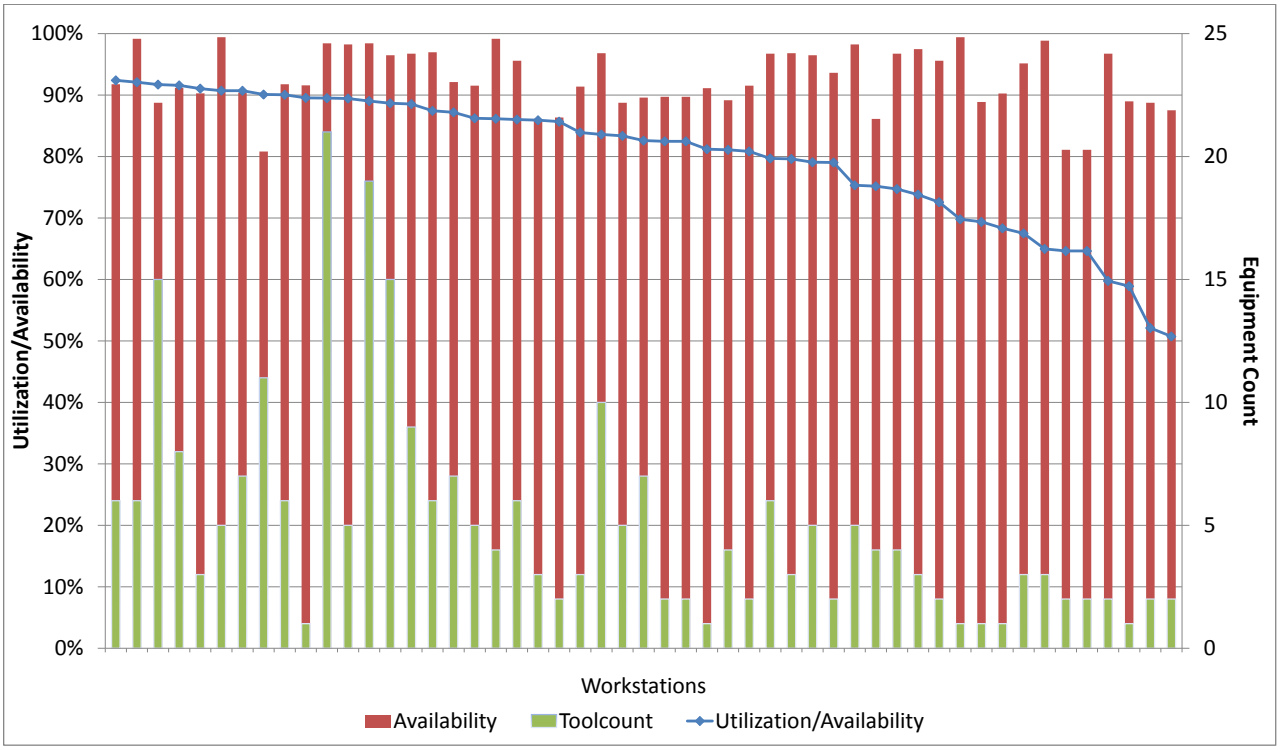

Figure 1: Utilization over availability chart for all workstations with toolcount at 92.5% fab loading.

specific characteristics in their dependance on lot size and toolset. We divide queue time into

- transport time (TT), denoting the time that lots travel between processing and storage locations,
- batch buidling and dissolving time (BT), denoting both the time spent waiting for other lots to form a process batch, and, the time spent waiting after the batch operation caused by the inability of following workstation to process all lots of the dissolved batch at once, and,
- remaining queueing time (QT), denoting the time spent waiting for a processing resource to become available.

We divide process time into

- processing time (t_0), denoting the time spent at the actual processing resource, and,
- delay (d) caused by the overlapping processing of consecutive lots often referred to as first wafer delay.

Figure 2: Cycle Time Components.

4 TOOLSET INCLUDING BATCH TOOLS

In this section we present our baseline model and assess which cycle time reductions are possible without changes of the toolset, i.e. the toolset includes a significant share of batch tools that process batches of many wafers. Batch tools perform all wet clean and most heat treatment operations in our baseline model accounting for about 38% of total non-metrology operations.

4.1 Baseline Model - Single Product Case

Figure 3 shows the cycle time results per component for the baseline scenario *Batch 24* and the derived lot size reduction scenarios *Batch 12, Batch 6, and, Batch 2* with *Batch* characterizing the toolset including batch tools and the numbers refering to the lot size of the scenario. The

lower and upper limit of the 95% confidence interval for total cycle time is within 1-2% of the average, therefore we do not show confidence intervals in any total cycle time chart.

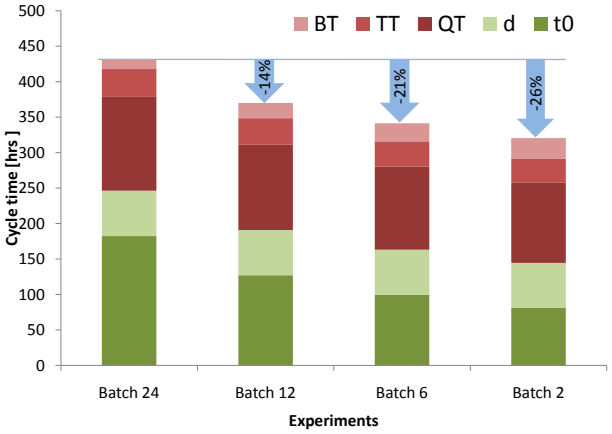

Figure 3: Lot size reduction scenarios for toolset including batch tools at 92.5% loading.

The cycle time of the baseline scenario equals 0.78 days per mask layer at an x-factor of 1.75. Such a performance is hardly achieved in today's fabs, however, we did not include all sources of variability into our simulation model. E.g. we exclude lot holds from our model which have a significant impact on cycle time, yet are independant from any of the discussed changes. Although cycle time performance of the baseline model is challenging, we judge this as a convincing baseline model for our research because the far-reaching changes of lot size reduction or tool replacements are only reasonable compared to well performing standard fabs. If a fab's cycle time performance could be significantly improved by conventional methods, then that would be more favorable in comparison.

In addition, Figure 3 shows cycle time improvements with lot size reduction. Total cycle time decreases by up to 26%, but it is difficult to see how the individual cycle time components contribute to this result. Therefore we show the relative change of all components in Figure 4.

- Processing time (t_0) is reduced most effectively because of the proportional relation to lot size for single wafer tools.
- Delay (d) does only change because of the increased lot skip rate at metrology operations. Due to the small d that lots encounter at metrology tools this results in hardly any change at all.
- Remaining queueing time (QT) decreases only slightly.
- Transport time (TT) decreases only because of the increased lot skip rate at metrology operations resulting in a slight total decrease.

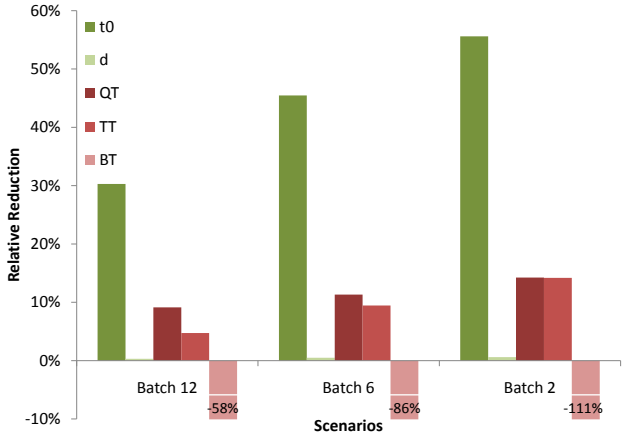

Figure 4: Reduction per cycle time component relative to baseline scenario at 92.5% loading.

- Batch buidling and dissolving time (BT) increases considerably with lot size reduction. However the total amount is not very significant, partially due to the one product setup.

In the following we want to highlight two interesting characteristics of the above experiments, the metrology cycle time and the batch building and dissolving time.

In Section 2 we presented our lot-size dependent sampling model which assumes constant total measurement times for all scenarios. As the model therefore incorporates a significant lot skip rate increase for metrology operations, cycle time decreases because much less lots actually see the operation. Figure 5 illustrates this reduction by showing the contribution of metrology tools to total process time and total queue time. The significantly reduced contribution for smaller lot size shows that cycle time of metrology operations is reduced very effectively outperforming the cycle time reduction at process operations.

The commonly used way to determine a batching time is by measuring the queue time of lots which have not formed a complete batch yet or by calculating it with a batching formula as in (Hopp and Spearman 2000). However, there is no such simple way to assess or calculate the batch dissolving time, especially when the dissolving process can stretch over several operations. Therefore we use an experimental approach. We additionally create a scenario having single wafer tool replacements for batch tools that have exactly the same availability and throughput rate characteristics as the corresponding batch tools. Of course, real single wafer tools would have different characteristics, therefore application of this scenario is limited to the experimental determination of BT. The resulting queueing time disadvantage of the batch scenario over the single wafer tool replacement scenario is our batch building and dissolving time BT'.

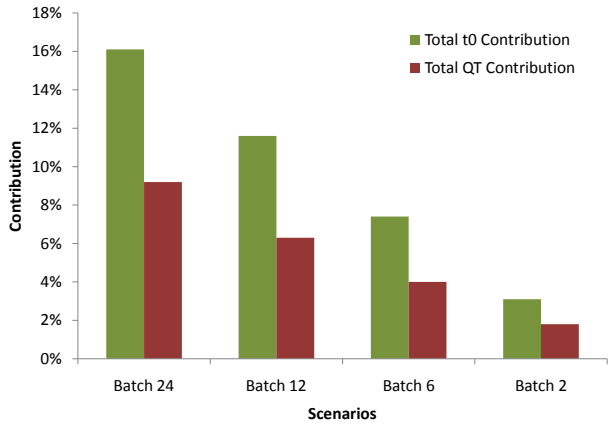

Figure 5: Contribution of metrology operations to total t_0 and QT at different lot size and 92.5% loading.

Figure 6 shows BT for the different lot size scenarios gathered by linear regression of BT'. BT decreases with increased fab loading and increases with lot size reduction.

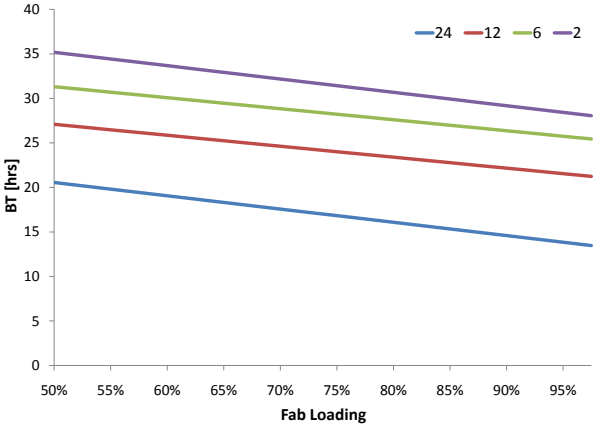

Figure 6: BT for different lot size at different loadings.

4.2 Multiple Product Case

In a modification of the baseline scenario, we assess the impact of a broader product spectrum on BT. In this scenario ten different products with an equal volume are processed. The ten products are started in full lots and round robin sequence and do not share the batching context, i.e., batches formed at batch tools do not contain lots of different products. The remaining processing specification is not changed, i.e. the products do not belong to a different technology.

Figure 7 shows the cycle time results of the multiple products scenario at different lot sizes compared to the baseline scenario at a lot size of 24 wafers. BT is significantly higher as in the baseline scenario. It does not increase ten times, though, because batches often do not fall completely apart between batch operations, they are just streamlined. It can also be seen that lot size reduction is less effective in terms of cycle time reduction for the multiple products scenario than for the one product scenario.

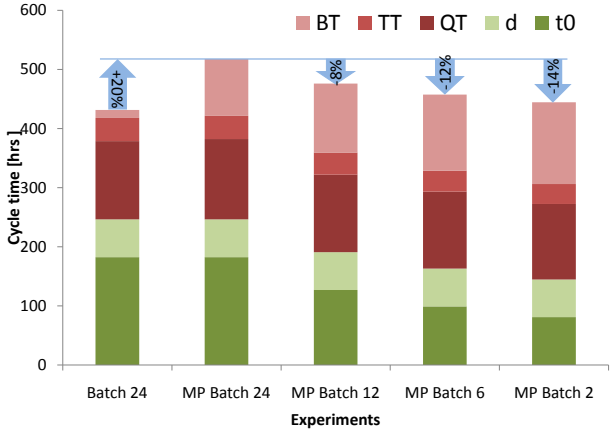

Figure 7: Lot size reduction scenarios for toolset including batch tools and multiple products compared to baseline model at 92.5% loading.

In this section we showed cycle time gains achieved by lot size reduction for a toolset including a significant share of batch tools. Most of the cycle time gained is due to a decrease in t_0 at single wafer tools which is partially offset by an increase in BT. Especially with multiple batching contexts this leads to an unconvincing cycle time performance considering the challenges involved with handling reduced lot size. Therefore lot size reduction with such a high share of batch tools seems unrealistic, perhaps with the exception of moderate lot size reduction and flexible batching contexts.

5 REPLACEMENT OF BATCH TOOLS

In this section we assess the cycle time improvement potential realized by replacing batch tools with mini-batch or single-wafer tools. Additionally we investigate how the cycle time reduction effectiveness of reducing lot size changes with this replacement. Both replacement scenarios are run with the baseline load of a single product. For a loading with multiple products, the cycle time improvement would increase in both cases compared to the batch scenario, as can be easily estimated by the different base size of BT.

5.1 Replacement with mini-batch tools

In our mini-batch scenario we replace all batch furnaces with corresponding mini-batch tools. The wet batch tools remain in the model, because there are no mini-batch tools for this application and batch size is already relatively moderate

with 50 wafers. (In our model the batch size is 48 wafers because of the different baseline lot size.) The mini-batch furnaces used in the simulation model all have a batch size of 24 wafers. Their throughput is oriented at existing mini-batch tools and is about half the throughput of the batch tools used in the model. As the original batch size is four times the mini-batch size, this means that t_0 is cut in half by this replacement at furnace operations.

Figure 8 shows the cycle time results of this scenario. Without any change in lot size the total cycle time is reduced by 14% by the furnace batch tool replacements. Already at this level of granularity it can be seen that BT is reduced very efficiently (by 167%) due to the higher baseline furnace batch size and fewer batching contexts shared between operations compared to wet batch operations. QT decreases slightly because of the increased tool count at the mini-batch workstations leading to less variance in the total available capacity. t_0 also decreases (by 16%) as derived above and d decreases by significant 27% caused by shorter loading times at mini-batch operations.

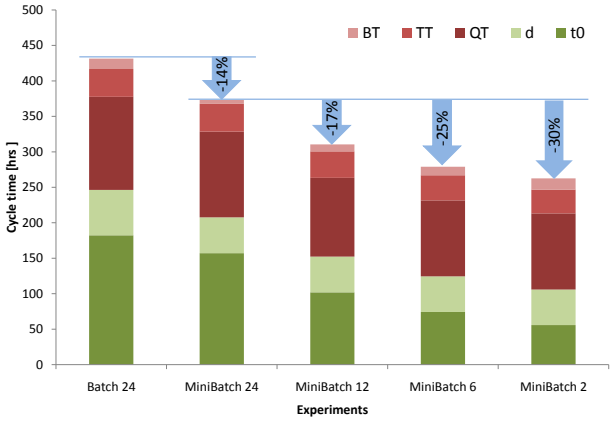

Figure 8: Lot size reduction scenarios for toolset converted to mini-batch tools compared to baseline model at 92.5% loading.

In the mini-batch scenario the switch to smaller lot size is slightly more efficient than in the baseline scenario because batch tools account for less cycle time at the 24 wafer lot. Additionally the mini-batch tools are less susceptible to negative cycle time impacts by different batch contexts because of the lower batch size. (Due to space constraints this is not shown here.) However, the cycle time reduction is far off the values realized with a pure single-wafer toolset in the following.

5.2 Replacement with single wafer tools

In our single-wafer tool scenario we replace all batch tools with corresponding single wafer tools. For most process applications of batch tools, corresponding single-wafer tools exist, but are not deployed because of worse cost of ownership. In these cases we use throughput and availability characteristics of existing tools for the replacements. If no corresponding single wafer tools exist to date, then we use the throughput of similar tools and applications. Whenever capacity of the single wafer tools requires tool additions or reductions, then we adjust the tool count accordingly.

Figure 9 shows the summarized cycle time results for the single-wafer toolset scenario. With the single-wafer tool replacements cycle time is reduced significantly by 24% compared to the baseline. Additionally lot size reduction is far more effective compared to the batch scenarios because improvements are effective across all workstations and there is no opposite effect from BT.

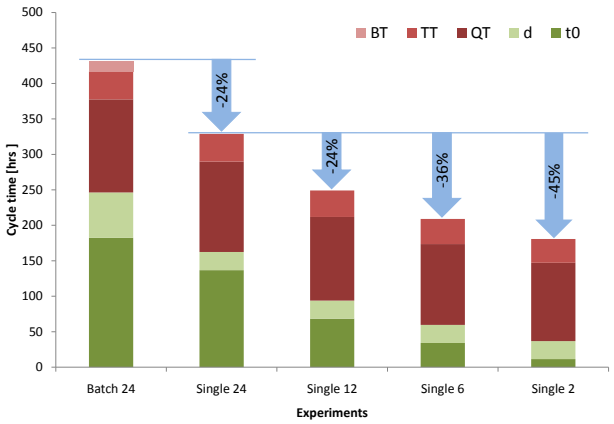

Figure 9: Lot size reduction scenarios for toolset converted to single wafer tools to baseline model at 92.5% loading.

Figure 10 illustrates additional details by showing the improvement per cycle time component.

- Processing time (t_0) is reduced by the switch to single-wafer tools and even more on because of the proportional relation to lot size for single wafer tools.
- Delay (d) does change significantly for the tool replacements because the long loading and unloading times of batch tools do no longer apply. Lot size reduction leads to hardly any change at all, again.
- Remaining queueing time (QT) decreases slightly for the switch in the toolset, mostly because additional tools are necessary due to lower single-wafer tool capacity and this decreases the variability in availability at these workstations with additional tools. Lot size reduction leads to an additional decrease, however, the decrease is not very significant for reductions below 12 wafers.
- Transport time (TT) is independent of changes in the toolset and with respect to the lot size reduction it changes exactly as for the batch scenario.

- Batch buidling and dissolving time (*BT*) does not occur in single-wafer tool scenarios, hence a reduction by 100% occurs.

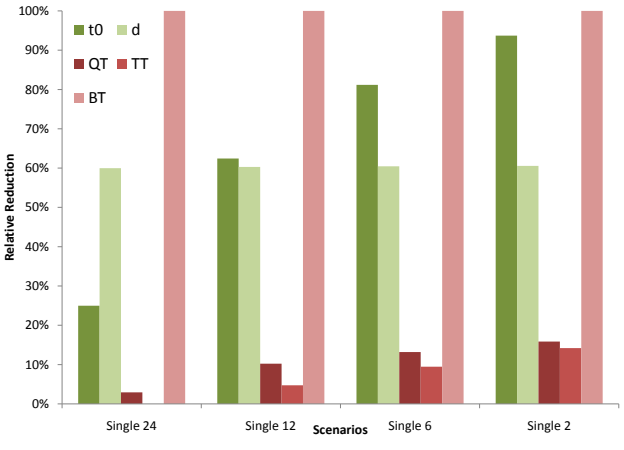

Figure 10: Reduction per cycle time component for toolset converted to single wafer tools relative to baseline scenario at 92.5% loading.

As the reduction in *QT* is not as straightforward as for the other components and is, in addition, utilization dependent (Schmidt and Rose 2007b), we take a closer look at the relative queueing time reduction in Figure 11. In this figure, we show the effect of lot size reduction by a comparison of Single 12 and Single 6 scenarios to the Single 24 scenario.

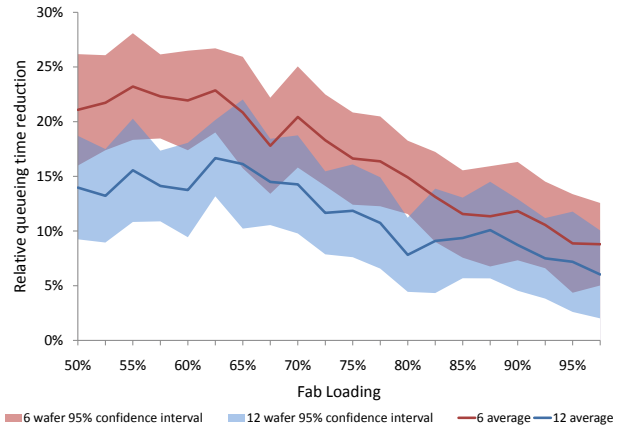

Figure 11: Relative queueing time reduction of 12 and 6 wafer lot size compared to 24 wafer lot size for pure single wafer toolset at different fab loadings.

We see that the relative queueing time reduction is much higher at lower utilizations. Under these conditions the negative impact of variability is less corrupting. It is also obvious that the reduction from 12 to 6 is less effective than from 24 to 12. This makes further reductions look unpromising. The 95% confidence interval reaches significant levels here, because variability impacts only this cycle time component and the graph shows a subtraction.

Figure 12 illustrates another interesting effect. So far we have shown the cycle time improvement by lot size reduction separately for different toolset scenarios and the effect of tool type replacement for 24 wafer lot size. In this case we show the cycle time improvement of tool type replacements starting at different lot sizes. The more the lot size is already reduced the more effective is a replacement. This also means that fabs running already at reduced lot size - for short cycle time or other reasons - replacements with mini-batch or single-wafer tools are even more promising.

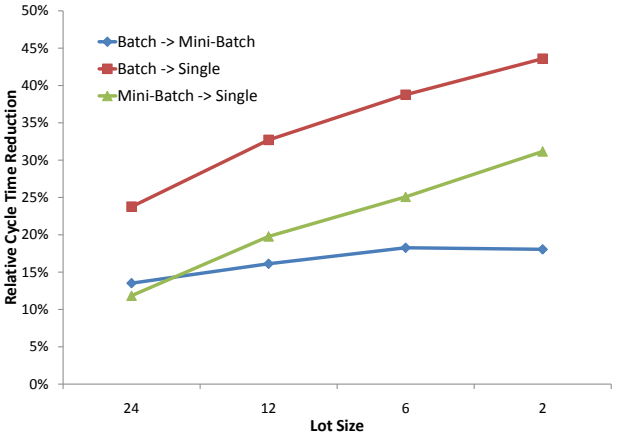

Figure 12: Cycle time improvement for toolset conversion at different lot sizes and 92.5% loading.

In this section we showed cycle time gains achieved by batch tool replacements and by lot size reduction for the new toolset. The batch tool replacements lead to a significant reduction in cycle time. The cycle time reduction effectiveness of lot size reduction is also significantly improved by the tool replacement. While 12 wafer lot size definitely looks promising for a pure single-wafer toolset, and 6 wafer lot size might be an interesting option in a fab with reduced variability characteristics, but further lot size reduction still lacks convincing effectiveness regarding the challenges involved.

6 SETUP CONSIDERATIONS

Setup times occur at some tools after a defined number of wafers have been processed or when process changeovers are necessary. Setups of the first type are usually clean processes that ensure a defined processing environment. Because of the defined interval they can be included in the processing times, and no major lot size dependent specifics are expected. However, setups of the second type can have an impact on the queue time decrease effectiveness of lot size reduction. Provided the number of different process

operations exceeds the number of tools at the workstation, then each queue time decrease has to go hand in hand with a reduction in the wafer cascade length denoting the number of wafers of the same recipe run back to back. This in turn means that setups happen more frequent, which decreases workstation capacity and leads to an increase in queue time. An example for these setups is beamtuning at implant operations that occurs with each process changeover. In our experience setups of this type other than beamtuning can be avoided by dedication provided a sufficient number of tools is available and this is the approach we have taken in our baseline model, ie. process changeover setups only occur at implant tools.

We embed our setup discussion into the single wafer scenarios. In this way, we have no difficulty in distinguishing between setup and batching effects, as both setup avoidance rules and batching per se lead to an agglomeration of lots at the same processing state. At all workstations with setups we use dispatching rules that avoid setups. In the following subsection we assess the setup impact at implant operations and in the next subsection we analyze the effect of additional setups when dedication is not used to minimize setups.

6.1 Setups in baseline model

Tables 2 and 3 summarize key figures detailing the effects of lot size reduction at both implant workstations. The low energy implant workstation of Table 2 has four tools serving seven operations and the high energy implant workstation of Table 3 has two tools serving three operations.

Table 2: Setup effects on queue time at low energy implant workstation at 92.5% fab loading

Lot size	Loading	Total QT	Setup state	Cascading
24	81%	4.94	6.6%	81.8
12	81%	4.87	9.6%	56.2
6	81%	4.80	12.4%	43.5
2	81%	5.07	14.4%	37.5

Table 3: Setup effects on queue time at high energy implant workstation at 92.5% fab loading

Lot size	Loading	Total QT	Setup state	Cascading
24	50%	0.79	6.9%	67.0
12	50%	0.72	11.1%	41.7
6	50%	0.75	16.4%	28.2
2	50%	0.80	23.3%	19.8

We want to highlight the following observations:

- The share of setup state increases and the wafer cascading length decreases significantly.
- Lower loading of high energy workstation leads to a higher increase in the share of setup state and to a sharper decrease in the wafer cascading length.
- The reduction in QT is far less than on average (see Figure 10) provided QT is reduced at all
- For very low lot size the QT increases.

6.2 Scenario with additional setups

In another scenario, we introduce additional setups by dissolving dedications. We combine three back-end etch workstations and two back-end cvd workstations to one workstation each. Because of the different process types performed within the workstation a 24 minute setup time is now necessary whenever the process type group is changed. Again, the dispatch rules at these workstations use an avoid setups policy and additionally a minimum number of tools per setup context is specified.

This setup scenario is quite different than the above example, because the number of setup contexts is significantly lower than the number of tools (three setup contexts at 22 etch tools and two setup contexts at seven CVD tools). Therefore there is no definite need that the setup frequency has to increase to enable queue time reduction.

Tables 4 and 5 display the total queueing time, the share of setup state per total time, and, the number of wafers that are processed between setups. In general the results confirm the observations made above at the implant workstations. However, the negative impact of setups is lower, e.g., the share of the setup state increases less with lot size reduction.

Table 4: Setup effects on queue time at etch workstation at 92.5% fab loading

Lot size	Loading	Total QT	Setup state	Wafers between setups
24	86%	3.30	1.7%	554
12	86%	3.03	2.0%	471
6	86%	2.99	3.3%	282
2	86%	3.04	4.6%	205

All examples show that setup times have a negative effect on the queueing time reduction aspired with lot size reduction. Limited occurence of setup times do not jeopardize the concept, however, as queueing time at affected workstation does not become considerably worse.

7 CONCLUSIONS

In this paper, we analyzed the effectiveness of two cycle time reduction approaches. Tool replacements with mini-batch or

Table 5: Setup effects on queue time at CVD workstation at 92.5% fab loading

Lot size	Loading	Total QT	Setup state	Wafers between setups
24	79%	3.97	4.3%	639
12	79%	3.77	6.0%	485
6	79%	3.68	8.6%	320
2	79%	3.75	10.2%	269

single wafer toolset show persuasive cycle time advantages especially for fabs with a diverse product portfolio that could be even higher in case of different technologies in the same fab. We also showed cycle time reductions for reductions in lot size. This approach, however, lacks persuasiveness if lot size is reduced to very small values. We have also shown that lot size reduction leads to less or no cycle time reduction at workstations with setup times, but this does not compromise the approach if setup times do not prevail. However, companies that consider lot size reduction have to evaluate how the extent of setups inherent to their product spectrum, tools and process capabilities influences the possible cycle time gain and seek opportunities to avoid setups efficiently.

In our future research we will analyze how hybrid solutions perform, ie. models which exploit small lot size only for some part of the flow, preferably the part with few or no batch tools. Additionally we will analyze equipment configuration or design possibilities that limit the variability impact and increase the effectiveness of cycle time reduction by smaller lot size.

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