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# ANALYSIS OF PRODUCTION CONTROL METHODS FOR SEMICONDUCTOR RESEARCH AND DEVELOPMENT FABS USING SIMULATION

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## ABSTRACT

A semiconductor company must bring technology to the market as soon as its application is deemed feasible to be a leader in the industry. The goal of this paper is to investigate production control methods in semiconductor R&D fabs to minimize the time to market for the aforementioned technology. Simulation models of a representative R&D fab are run with different levels of bottleneck utilization, lot priorities, primary and secondary dispatching strategies and due date tightness as treatment combinations in a formally designed experiment. The fab performance measures are percent on time delivery, average cycle time, standard deviation of cycle time and average work-in-process. Fab characteristics are found to influence the application of dispatching rules. However, several dispatching rules are found to be robust across performance measures.

## 1 RESEARCH AND DEVELOPMENT IN SEMICONDUCTOR R&D FABS

The invention of the transistor in 1947 served to make semiconductors, the leaders of the electronics revolution (Busch 1999). An article on the top 100 R&D spenders in the IEEE Spectrum publication ranks International Business Machines Corp., U.S. and Intel Corp., U.S., major players in the semiconductors and semiconductor equipment sector, in the top 15 (Hira 2003). The semiconductor industry ranks behind only the automotive and communications industries in annual R&D spending. In 2001, the industry spent $14.2 billion on R&D (Wolfe 2002). The industry falls into the category of high technology because a high proportion of these R&D costs as a percentage of sales and also because a high number of the employees are scientists and engineers (Green 1996).

Technology and product development are key to the success of semiconductor manufacturers. Thus, most of the industry leaders have both production fabs, where products are made for sale to the public, and research and development (R&D) fabs, where new technologies and products are designed and tested. Although production fabs and R&D fabs may have similar tool sets, semiconductor production fabs operate differently than R&D facilities. These differences arise from the scales of production, lot prioritization, material handling techniques and performance parameters. Production fabs aim at increasing throughput for maximizing profits whereas R&D fabs concentrate on developing new technology and minimizing time to market.

Production fabs in general are characterized by a low product mix, high production volumes, established products with standardized routings and established processes. On the other hand, R&D fabs are characterized by large product mix with unique and/or non-standard routes, prioritization of research activities, random engineering holds and mandatory testing procedures.

While a significant body of research exists for designing, analyzing and improving the performance of production fabs, very little has been done to study the performance of R&D fabs. In general, this paper involves conducting simulation experiments on models of R&D fabs to determine factors that significantly effect fab performance and focuses on performance improvement in terms of due date and cycle time performance. Furthermore, prioritization policies are investigated, that are encountered in R&D fabs.

## 2 PROBLEM DEFINITION AND OBJECTIVES

To gain a large share of the market, a semiconductor company needs to minimize time to market to make its technology commercially available faster than its competitors. This is essential for a company to maximize profits (Johal 1998). Minimizing time to market can be achieved by shorter cycle times in the various stages of new product development, which include the concept design, the detailed design and the production of prototypes. This paper

investigates production control methods in semiconductor R&D fabs. The appropriate use of which will enable a faster transfer of technology to the production fabs. This in turn reduces the time to make the product commercially available.

The product and process development phase is one of the most complex and expensive steps in semiconductor manufacturing. With advent in technology, Very Large Scale Integration (VLSI) allows for more and more chips to be integrated into the wafer. A significant reinvestment of revenue goes into supporting R&D fabs to maintain these technological advances in the semiconductor industry. R&D fabs operate differently than production fabs. R&D fabs may host several processes and products at varying WIP levels and priorities. Hindrances to process flow like random stoppages, tool reservations and lot prioritization are inherent characteristics of R&D fabs. This study investigates methods to increase productivity and quantify the performance of semiconductor R&D fabs considering the influence of hot lots or high priority lots using system simulation with a focus on employing production control.

A simulation model of a representative R&D fab is built using a representative load to approximate production with priorities assigned to wafer lots. The lots have three classifications of priorities; H, M and L, where H is high priority, M is medium priority and L is low priority. The model is simulated according to treatment combinations of a formally designed experiment. The factors of this experiment are bottleneck utilization, primary/secondary dispatching rules, due date tightness and product mix. Dispatching rules including Priority, FIFO, Critical Ratio, Highest X-Theoretical Ratio First and Least Balance Ahead are used as primary and secondary rules. This covers the four classifications of dispatching strategies that are based on processing time, due dates, strategies based on neither processing time nor due date and finally a combination of the three strategies (Sha and Hsu 2004). This helps compare the use of employing different dispatching rules. The use of statistical analyses helps compare the performance of the different dispatching rules. Fab performance is reflected by the behavior of the performance measures, which are percent on time delivery, average cycle time, standard deviation of cycle time and average WIP.

## 3 RELATED WORK

Related research on improvements in semiconductor R&D fab productivity has focused on cycle time reduction strategies using simulation and management approaches (Janakiram 1996), the use of simulation to evaluate the use of conventional dispatching rules to fab behavior (Tullis et al. 1990), investigation of cycle time metrics to relate cycle time to fab behavior (Pierce et al. 1995) and the development of scheduling tools specifically catered towards the production uncertainties of R&D fabs (Liao et al. 1995, Shiu et al. 1996, and Lu et al. 1994).

Past research on improvements in semiconductor production fab productivity has focused on asserting the differences in impact of scheduling depending on factors like the nature of the fab and presence of hot lots (Wein 1988), evaluating the effects of hot lots to semiconductor fab productivity and analyzing their impact to fab behavior using simulation (Domaschke et al. 1998), studying the effects of priority lots using mean value analysis (Narahari and Khan 1997), and using object oriented simulation to study the impact of "hot lots" of cycle time on other lots (Ehteshami et al. 1992).

## 4 SIMULATION OF REPRESENTATIVE SEMICONDUCTOR R&D FABS

In this section, models of representative semiconductor R&D fabs are that are built and analyzed as part of the experimental design are discussed. The sub-sections detail the modeling assumptions and description of the setup of the simulation software package used for the simulation. The modeling assumptions include the constraints, operator actions, and tool certifications for technicians.

### 4.1 Simulation Model Assumptions and Details

The Complementary Metal Oxide Semiconductor (CMOS) recipe is chosen as the routing for the representative wafer lots. This recipe comes closest to matching the average tool usage in the SMFL. This ensures that the routing loads the fab like the actual tool usage in the fab. The constraints that stop these lots from processing on the tools are:

- Tool reservations;
- Down events;
- PM events;
- Off shift events; and
- Waiting times.

Tools are reserved for researchers with specific requests. Other researchers can use tools and other fab facilities during reserved hours. Shift calendars dictate the availability of fab personnel.

Priority-designated lots are introduced into the fab. These lots have three different classifications viz. H (high), M (medium) and L (low) lots.

A researcher spends 8 hours in the fab, Mondays through Fridays, from 8 am to 4 pm. The model also has preemption provisions. The researcher will not put a lot on his worklist unless he has sufficient time on hand to process the lot. For e.g. the LPCVD tool requires a total processing time of 220 min and a lot has the LPCVD operation in the next step of its route. The researcher will not process

the lot unless he has the full 220 min available before his shift ends.

Action lists in the model provide sets of instructions or actions for task performance by the schedulable entity. Steps in the route either require a researcher to be present:

- for setup only; and
- for setup and processing.

Custom action lists are made and associated with the steps in the route, according to their need for researchers as above.

Technical operators are dedicated to PM events and down times for tools. These operators are available Mondays through Fridays from 8:30 a.m. to 4 p.m. The model has a total of 5 technical operators with different certifications. The certifications are shown in Table 1.

Table 1: Tool Certifications for Technicians

| Technical Support | Tool Certification | Processing Efficiency |
|---|---|---|
| Tech. Worker 1 | ASM LPCVD | 1.00 |
| | Branson Asher | 0.66 |
| | Drytek RIE | 1.00 |
| | Bruce furnace tubes | 0.66 |
| Tech. Worker 2 | LAM 490 Plasma etch | 1.00 |
| | Varian 350D Implanter | 1.00 |
| | CVC-601 Sputter | 1.00 |
| Tech. Worker 3 | RCA Clean | 1.00 |
| | Canon & GCA Steppers | 1.00 |
| | Bruce furnace tubes | 1.00 |
| Tech. Worker 4 | RCA clean | 0.66 |
| | Branson Asher | 1.00 |
| | Varian 350D Implanter | 0.66 |
| Tech. Worker 5 | RCA clean | 0.66 |
| | Drytek RIE | 0.66 |
| | LAM 490 Plasma etch | 0.66 |
| | Varian 350D Implanter | 0.66 |
| | ASM LPCVD | 0.66 |

The primary technician has a higher processing efficiency than the secondary technician. The secondary technicians operate at 2/3 times the efficiency as the primary technicians on the concerned tools. The secondary technician works on the tool only if the primary technician is busy or unavailable. PM events never interrupt a resource from processing a wafer lot. The scheduled PM comes into effect once the resource finishes processing on the lot. All resources in the fab including the technical operators have a capacity of 1. This means that they can process only one entity at a time.

### 4.2 Simulation Software Setup

The representative semiconductor R&D fab is simulated using Brooks Automation's Autosched AP (ASAP), a discrete-event simulation software package. Autosched AP, a finite capacity planning and scheduling tool is used to model the working of factories. The factory's real system terms are translated into model terms

ASAP uses worksheets to allocate stations, routes, orders, parts and storage. The categories of data essential for model creation are resources, products and demands. These data sets can be imported from other databases or from the shop floor control system. (Phillips 1998).

### 4.3 Verification and Validation

Once the simulation model is built, verification is done to ensure that the AutoSched AP model runs as is intended. The software package includes a message file that can be read at the end of every simulation run. Events are traced in the message file and this allows for the user to conduct verification steps such as walkthroughs and checking for errors. This message file feature is used to authenticate the modeling of end of shift effects, technician certification and tool downtime and PM events.

After the verification process, the model is validated to ensure that it adequately represents a semiconductor R&D fab. Discarding outliers and suspicious entries and walkthroughs with experts validates data on stations, routings, process and setup times, pulled from the Camstar Manufacturing Execution System Application (MESA) database at RIT. Information on down times, preventive maintenance (PM) events and statistics on distributions for these events are obtained by compiling empirical data from the MESA. All the data and the information are validated as exclusive to typical semiconductor R&D fabs. The specific characteristics may differ from fab to fab but essential characteristics like down times, PM events, single shifts and the representative product load that are built into the model are representative of semiconductor R&D fabs.

## 5 THE SIMULATION EXPERIMENT

The experiment conducted, as part of the methodology to analyze production control methods, tests different levels of production volume, primary/secondary dispatching rules, due date tightness and product mix. Fab performance is quantified by performance measures including percent on time delivery, average cycle time, standard deviation of cycle time and average WIP. Running a simulation model of a semiconductor R&D fab with different levels of pertinent factors enables fab managers to use the best dispatching rules to minimize time-to-market.

The objective is to find out which of the dispatching rules tested are the most robust. This means that they can

be applied to a given semiconductor R&D fab, without a huge cycle time/on time delivery trade off. Also certain dispatching rules may perform better than others according to the prevalent operating conditions of the fab. The analysis of the results give a clear picture as to what rules can be applied for different scenarios. The experiment also checks if the effect of the application of different dispatching strategies has statistical significance on percent on time delivery, average cycle time, standard deviation of cycle time and average WIP.

### 5.1 The Experimental Design

A formally designed experiment is run with the factors being bottleneck utilization (BU), dispatching rules (DR), due date tightness (DDT) and product mix (PM). Table 2 shows the factors and their levels.

Dispatching rules consist of primary and secondary rules, in the format primary/secondary and the Product Mix which is the ratio of high, medium and low priority lots is given in the format H-M-L.

Table 2: The Design of Experiments

| Factors | Levels |
|---|---|
| Bottleneck Utilization (BU) | High and Low |
| Dispatching Rules (DR) | P/FIFO, FIFO, CR/FIFO, HXT/FIFO, P/CR, P/HXT and LBA/FIFO |
| Due Date Tightness (DDT) | Tight Flow Factor (TFF) and Relaxed Flow Factor (RFF) |
| Product Mix (PM) | 25-25-50, 15-15-70 and 5-5-90 |

Bottleneck Utilization (BU) is used as a factor in the experimental design to vary the production volume in the fab. Semiconductor R&D fabs are characterized by differing levels of production volumes. It is important to vary the levels of the volumes to test for significance of this factor. Having lots enter the fab at constant average interarrival rate levels of 57 hours and 68.4 hours controls the production volume. At a constant average interarrival rate of 57 hours, the bottleneck tool has a utilization of between 95% and 99%. The total lot starts amount to 154 lots/year. This is the high level of BU. A constant interarrival rate of 68.4 hours sees a reduction in lot starts by 20% and this will indirectly ease the bottleneck utilization. Here, the number of lot stars amount to 128 lots/year. This is the low level of BU. The lot start rates for the different classification of priority-designated lots always average to the desired level of the production volume. For e.g. for a product mix of 50% L lots, 25% M lots and 25% H lots, the lots start rates are 114 per hour, 228 per hour and 228 per hour respectively. This means that in a time window of 228 hours, 4 lots enter the fab with a constant average interarrival rate of 57 hours.

Dispatching rules (DR) are used to rank wafer lots in resource worklists according to chosen lot attributes. These attributes may be time, due date or priority based or any combination of these. The dispatching rules used in this research are FIFO, Priority-based, Critical Ratio, Highest X-Theoretical Ratio first and Least Balance Ahead. The FIFO, Critical Ratio and Highest X-Theoretical Ratio rules are also used in conjunction with the Priority-based rule as secondary dispatching rules. Secondary dispatching rules break a possible tie between lots ranked by the primary dispatching rule. Here is a brief description of the dispatching rules used in this research:

- **The Priority Dispatching Rule (P)**: ranks lots on resource worklists according to the processing priority associated with the lot (H>M>L).
- **First-In-First-Out (FIFO)**: ranks lots according to their order of arrival on resource worklists. It treats lots on a first come first serve basis.
- **Critical Ratio (CR)**: ranks lots according to the lowest Critical Ratio first and is calculated

$$\text{Critical Ratio} = \frac{(\text{Time Unil Due})}{(\text{Remaining Processing Time})}.$$

- **Highest X-Theoretical Ratio First (HXT)**: ranks lots according to the highest X-Theoretical Ratio first and is calculated

$$\text{X - Theoretical Ratio} = \frac{(\text{Total Time in System})}{(\text{Theoretical Process Time})}.$$

- **Least Balance Ahead (LBA)**: ranks lots according to the least number of lots of the same part type in the next step in the route.

Due Date Tightness (DDT) levels are laid down using flow factors, which are multiples of the raw or theoretical processing times. Flow factor multiplied by the raw processing time gives the target cycle time or lead time (Rose 2002). The simulation software used, then calculates the due date for every lot by the estimated lead-time entered for the product. This due date critically affects the behavior of the CR rule, which is a due date based rule. The raw processing time for a wafer lot in the representative CMOS route is 83 hours. Two levels of target cycle times or due dates for each priority classification are tested. The first level employs due date tightness at 20, 15 and 10 times that of the raw processing time for low, medium and high priority lots respectively. This is the Tight Flow Factor (TFF) level of DDT. The second level tests these lots for on time delivery at 25, 20 and 15 times the raw processing time.

This is the Relaxed Flow Factor Level (RFF) of DDT. These levels have been set taking into consideration the priorities of the lots and the urgency associated with these priorities.

Three levels of lot start percentages are used in order to vary the product mix (PM) on the fab floor. The L lots are tested at levels of 50%, 70% and 90% of the total lots with the remaining proportion being equally distributed between M and H lots. In semiconductor R&D fabs, the definition of priority-designated lots may tend to differ. Ehteshami et al. (1992), test the effects of these lots in ranges varying from 0% to 16.7%. While this is true for semiconductor production fabs, this proportion may be exceeded in R&D fabs. In R&D fabs, high priorities may be assigned to lots based on the urgency and nature of the research and the lots' path in the product development cycle. This research assumes that the combined proportion of medium and high priority-designated lots in the route may not exceed 50% of total lots in the system.

### 5.2 Performance Measures

The performance measures analyzed in this study are the average cycle time, standard deviation of cycle time, percent on time delivery and average WIP. These parameters reflect fab behavior and have been used widely for that purpose.

The semiconductor R&D fab modeled as part of this research operates one shift per weekday. The length of this shift varies from 8 to 10 hours per day. This means that all the above performance measures include the shelf times or the non-operational times of the fab. This is one reason that the flow factor is high as compared to those used for conventional production fabs. For e.g. if the fab shuts at 4 pm on a Monday and opens on 8 am on Tuesday, the lot cycle time will include the time spent by the lot in the state between the 4 pm on Monday and 8 am on Tuesday. It is important not to exclude this time from the performance measures since a characteristic of semiconductor R&D fabs is non-contiguous shifts.

The lot cycle time is hence defined as the total time taken by the lot to traverse from the lot start to the end of the product route. The Average Cycle Time averages the cycle times of the lots that make it out of the fab. The percentage on time delivery depends on the lots abiding by the set due dates. The average WIP is the number of lots in process or on the worklist of resources at any given time in the fab during the simulation run length.

### 5.3 Statistical Analyses Procedures

The goal of this paper is to determine which dispatching rules, due date tightness levels and/or combinations of the two are most suited to different levels of production volumes and production mixes. To come up with these results, detailed statistical analyses are required. The analyses are done using the statistical software program MINITAB after compiling the simulation results.

Based on previous research, it is expected that the factors tested in this research are significant. An ANOVA (Analysis of Variance) test is conducted on all the four factors to determine whether the main effects and the interaction effects are significant. The level of confidence for the factor significance is set at 95%. All the factors and their interactions are expected to be significant. This leads to a three factor investigation of dispatching rules, due date tightness and product mix for each of the two levels of production volume. These factors and their interactions are again expected to be significant. This leads to a two factor analyses which tests dispatching rules and due date tightness at every combination of production volume and product mix level. These analyses are especially important since the results will show the best combination of dispatching rules and due date tightness for a given R&D fab. The results are particularly useful when the due dates are not a controllable factor in fabs. The fab manager can instantly decide a production control strategy if the determination of due dates is beyond his control. Depending on whether the two factor interactions or the main effects are significant, Tukey pairwise comparison tests are done to determine which factor levels are statistically significant from each other. After the two factor analyses and Tukey Tests are done, it becomes possible to list the combination of dispatching rules and due date tightness that perform the best for each level of product mix at each level of production volume.

The last set of analyses test the performance of dispatching rules by using production volume, product mix and due date tightness as controlling factors. Again, ANOVA tables are analyzed for the significance of the main effect and Tukey Tests are conducted. A summary table gives the top group of dispatching rules for each fab type.

## 6 RESULTS

This section discusses the results from the statistical analyses performed. The analysis of all factors and their interactions is conducted via ANOVA tables, where it is seen that the majority of the factors and their interactions are significant for the four performance measures at $\alpha$=0.05. All the factors and their interactions are significant at this level of confidence for the percent on time delivery performance measure. DDT, PV*DDT, DR*DDT, DDT*PM, PV*DR*DDT and PV*DDT*PM are not significant at this level for average cycle time, standard deviation of cycle time and average WIP.

An analysis of factors and their interactions for dispatching rules, due date tightness and product mix with given levels of production volume is performed and it is

seen that for high bottleneck utilizations, all factors and their interactions are statistically significant for the percent on time delivery performance measure at α=0.05. DDT and DR*DDT are not statistically significant for average cycle time, standard deviation of cycle time and average WIP and DDT*PM is not statistically significant for average cycle time and average WIP at the same level of confidence. For low bottleneck utilizations, all factors and their interactions are statistically significant for the percent on time delivery performance measure at α=0.05. Only the DDT*PM and DR*DDT*PM interactions are not significant at the same level of confidence for average cycle time, standard deviation of cycle time and average WIP.

### 6.1 Analysis of Dispatching Rules and Due Date Tightness

The three factor ANOVA results are used as the basis for conducting a two factor ANOVA with the factors being dispatching Rules and due date tightness for each product mix level at each bottleneck level. Table 3 shows that for the percent on time delivery response, all factors and their interactions are significant at a confidence level of 95%.

Table 3: ANOVA Table for % On Time Delivery at High BU and PM = 25-25-50

| Source | DF | Seq SS | Adj SS | Adj MS | F | P |
|---|---|---|---|---|---|---|
| **DR** | 6 | 23693.3 | 23693.3 | 3948.9 | 2648.6 | 0.000 |
| **DDT** | 1 | 2565.0 | 2565.0 | 2565.0 | 1720.4 | 0.000 |
| **DR*DDT** | 6 | 790.0 | 790.0 | 131.7 | 88.3 | 0.000 |
| **Error** | 28 | 41.7 | 41.7 | 1.5 | | |
| **Total** | **41** | **27090.0** | | | | |

Table 4 shows the Tukey comparison for the combination of Dispatching Rules and Due Date Tightness for percent on time delivery. The vertical lines in the significance column group the strategies that are not statistically different from each other. In Table 4, the FIFO and RFF combination is not statistically different from the LBA/FIFO and RFF combination but is statistically different from the HXT/FIFO and RFF combination. FIFO and LBA/FIFO at a relaxed due date tightness level for the H, M and N lots perform well.

Similar ANOVA tables and Tukey tables are constructed for the other levels of product mix at each level of bottleneck utilization.

Tables 5 and 6 list the top groups of combinations of dispatching rules and due date tightness strategies at high and low levels of bottleneck utilizations respectively at the three levels of product mix. The rules that have been named robust in most cases perform well for percent on time delivery, average cycle time and average WIP. The standard deviation of cycle time measure gives an indication of the consistency of the average cycle time of the lots in the fab. Hence rules find themselves as being robust even if they don't make it to the top group for the standard deviation of cycle time performance measure.

Table 4: Tukey Pairwise Comparison Test for % On Time Delivery for High BU and PM=25-25-50

| Dispatching Rule | Due Date Tightness | % On Time Delivery | Significance |
|---|---|---|---|
| FIFO | RFF | 86.34 | |
| LBA/FIFO | RFF | 85.21 | |
| HXT/FIFO | RFF | 71.13 | |
| FIFO | TFF | 66.05 | |
| LBA/FIFO | TFF | 64.61 | |
| P/CR | RFF | 50.31 | |
| P/HXT | RFF | 50.11 | |
| P/FIFO | RFF | 49.86 | |
| HXT/FIFO | TFF | 41.31 | |
| P/FIFO | TFF | 39.41 | |
| P/HXT | TFF | 37.25 | |
| P/CR | TFF | 34.92 | |
| CR/FIFO | TFF | 0 | |
| CR/FIFO | RFF | 0 | |

Table 5: Top Groups of Strategies for High BU

| Product Mix | Robust Strategies Across Performance Measures |
|---|---|
| 25-25-50 | FIFO@RFF<br>LBA/FIFO@RFF |
| 15-15-70 | P/FIFO@RFF |
| 5-5-90 | P/FIFO@RFF<br>P/HXT@RFF |

Table 6: Top Groups of Strategies for Low BU

| Product Mix | Robust Strategies Across Performance Measures |
|---|---|
| 25-25-50 | P/FIFO@RFF<br>P/HXT@RFF<br>FIFO@RFF |
| 15-15-70 | P/FIFO@TFF<br>P/FIFO@RFF<br>P/HXT@TFF<br>P/HXT@RFF<br>LBA/FIFO@RFF<br>FIFO@RFF<br>HXT/FIFO@RFF |
| 5-5-90 | HXT/FIFO@RFF<br>LBA/FIFO@RFF<br>P/HXT@TFF<br>P/HXT@RFF<br>FIFO@RFF |

The FIFO, P/FIFO and P/HXT rules perform well at a relaxed due date tightness level for both levels of bottleneck utilization. It is interesting to observe that the due date based rules, CR/FIFO and P/CR do not make it to the top groups for both levels of production volume.

### 6.2 Analysis of Dispatching Rules in Specific Fab Types

By using due date tightness as a controllable factor, dispatching rules can be examined individually, as to what rules work best given a certain operating condition in the fab. In this case, the bottleneck utilization, product mix and due date tightness are all used to generate 12 fab types. This is done to give fab managers a good indication as to what dispatching rules work best for given operating conditions. Table 7 lists the levels of production volume, due date tightness and product mix under which each fab operates.

Table 7: Fab Type by Operating Condition

| Fab Type | Bottleneck Utilization | Due Date Tightness | Product Mix (lot start percentages - H-M-L) |
|---|---|---|---|
| **I** | High | TFF | 25-25-50 |
| **II** | High | RFF | 15-15-70 |
| **III** | High | TFF | 5-5-90 |
| **IV** | High | RFF | 25-25-50 |
| **V** | High | TFF | 15-15-70 |
| **VI** | High | RFF | 5-5-90 |
| **VII** | Low | TFF | 25-25-50 |
| **VIII** | Low | RFF | 15-15-70 |
| **IX** | Low | TFF | 5-5-90 |
| **X** | Low | RFF | 25-25-50 |
| **XI** | Low | TFF | 15-15-70 |
| **XII** | Low | RFF | 5-5-90 |

ANOVA and Tukey tests are conducted for all 12 fab types for all four performance measures. Table 8 lists the top groups of dispatching rules for every fab type for every performance measure.

For the levels of product mix with lower proportions of low priority designated lots, it is seen that the FIFO and LBA/FIFO rules perform the best. The P/FIFO and P/HXT rules perform better for the lower level of production volume and for product mixes with higher proportion of low priority-designated lots. It is interesting to note that from the Tukey tables, the due date based rules, CR/FIFO finds it self in the top group of almost all fab types for the percent on time delivery but is not a robust rule across other performance measures. Similarly, the HXT/FIFO rule performs consistently well for the standard deviation of cycle time performance measure for most fab types but is a robust rule only for two fab types.

Table 8: Analysis of Dispatching Rules for the 12 Fab Types

| Fab Type | Robust Strategies Across Performance Measures |
|---|---|
| **I** | FIFO<br>LBA/FIFO |
| **II** | P/FIFO |
| **III** | P/FIFO<br>P/HXT |
| **IV** | FIFO<br>LBA/FIFO |
| **V** | LBA/FIFO |
| **VI** | P/FIFO<br>P/HXT |
| **VII** | P/FIFO<br>P/HXT<br>P/CR |
| **VIII** | HXT/FIFO<br>P/FIFO<br>P/HXT |
| **IX** | P/HXT |
| **X** | P/CR<br>P/FIFO<br>P/HXT |
| **XI** | P/FIFO<br>P/HXT |
| **XII** | HXT/FIFO<br>LBA/FIFO<br>P/HXT |

### 6.3 Performance of the Due Date Based Rules

From the results in Tables 5, 6 and 8 it is clear that the CR/FIFO rule does not perform well across all the performance measures. The CR/FIFO performs well for the percent on time delivery response but fails to perform consistently well over the other measures. The P/CR rule is a robust rule for only one of the twelve fab types. It is seen from the raw data that the CR/FIFO rule has extremes when it comes to percent on time delivery with value of either 0% or grater than 96%. The P/CR rule does not do very well when compared to the other rules. The CR/FIFO rule performs better than the P/CR rule for average cycle time but does poorly when compared to the other robust rules. A few reasons for this unexpected behavior of the due date based rules maybe:

- Lots with high slack remain at the bottom of resource worklists to give way to lots with lesser slack;
- Newer lots with high slack always give way to older lots with lesser slack;
- High numbers of reentrant steps, characteristic to semiconductor process routes hinder lot progress on account of slack and/or priority; and

- Due date based rules exclusively cater to giving precedence to lots with least slack and hence for higher volumes of production or higher proportions of one level of priority, lots will often have negative slack because of waiting on resource lists for processing. On the other hand, when due date based rules give good percent on time delivery values for certain fab scenarios, tend to balance out the average cycle time among the many products in the fab. These average cycle time values are not as high as some other rules. This is where the due date rules lose out on being robust because there is no good tradeoff between on time delivery and cycle time.

## 7 SUMMARY OF EXPERIMENTS

A formally designed experiment tests levels of production volume, product mix, dispatching rules and due date tightness at different levels via a simulation model of a semiconductor R&D fab. High, medium and low are the three levels of priority-designated lots introduced in the fab. The performance measures for production strategy evaluation are percent on time delivery, average cycle time, standard deviation of cycle time and average WIP. Production strategies are evaluated first by assigning production volume and product mix as controllable factors. It is observed that the due date based rule, CR/FIFO, performs well for product mixes where there are larger numbers of low priority-designated lots at a relaxed level of due date tightness. Although this rule does not find itself in the top groups for the average cycle time performance measure, it helps reduce the time to market for the fab products. Due date tightness then is assigned as a controllable factor and dispatching rules are evaluated according to 12 fab types with different levels of production volume, product mix and due date tightness. Again it is observed that the CR/FIFO rule performs well for fabs with lower proportions of medium and high priority-designated lots for the percent on time delivery performance measure. FIFO, LBA/FIFO, P/FIFO and P/HXT are observed to be the most robust dispatching rules across performance measures.

## 8 CONCLUSIONS

Semiconductor Research and Development fabs feed the technology to semiconductor production fabs for commercial large-scale manufacturing. It is essential that this technology be transferred to the production fabs on time so as to be on par if not beat the competition. In other words, the time to market the technology has to be as short as possible. Previous research has touched on the prevalent conditions of semiconductor R&D fabs and improvement from a project management approach but not focused on the important issue of analyzing production control methodologies and strategies for semiconductor R&D fabs. This research involves understanding the behavior of semiconductor R&D fabs and evaluating fab specific production control methods to increase productivity by shortening the time to market of the products.

From the statistical analyses conducted from the simulation results, it is seen that the due date based rule CR/FIFO works well for the percent on time delivery response in most fab scenarios but fails to be a robust rule across all performance measures. The robust rules across performance measures are found to be the FIFO, LBA/FIFO, P/FIFO and P/HXT rules. The CR/FIFO rule can still be used as an effective dispatching rule to get the best percent on time deliveries but at the cost of cycle time of the lots in the fab. It works best in scenarios where the proportion of low priority-designated lots outweighs the proportion of medium and high priority-designated lots. The P/FIFO and P/HXT rules work best for all performance measures except when there is a heavy volume of production. In such cases the FIFO and LBA/FIFO prove to be robust rules.

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