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# SIMULATION BASED CAUSE AND EFFECT ANALYSIS OF CYCLE TIME AND WIP IN SEMICONDUCTOR WAFER FABRICATION

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## ABSTRACT

Semiconductor wafer fabrication is perhaps one of the most complex manufacturing processes found today. In this paper, we construct a simulation model of part of a wafer fab using ProModel® software and analyze the effect of different input variables on selected parameters, such as cycle time, WIP level and equipment utilization rates. These input variables include arrival distribution, batch size, downtime pattern and lot release control. SEMATECH DATASET which has the original actual wafer fab data is used for our analysis.

## 1 INTRODUCTION

Today's semiconductor industry is more dynamic and competitive than ever. Product's profit cycles are shrinking quarterly. Products that used to have a life cycle of 18 months now have average profit cycle of only 6 months. Customer demand for shorter cycle times and specialized packaging/delivery requirements is an obvious major trend. The entire semiconductor industry is very sensitive to the economic and trade climates. It is typical in the semiconductor market to have large oscillations in demand. Additionally, in semiconductor manufacturing, the number of operations in production routes is large, and due to the trade-off of waiting time in exchange for high equipment utilization in a factory of unreliable equipment, cycle time is long in general.

It is obvious that there are many benefits of reducing the mean cycle time. In general, a small cycle time improves the company's ability to respond to changing customer demands, and reduces the work-in-process inventory for any given level of throughput. Reducing the variance of the cycle time is more important as it leads to better prediction of the completion time of the product and it is critical for accurate planning and due-date assignment. This facilitates improved coordination of up/ down stream operations on the products. Besides cycle time, there are other main parameters in semiconductor manufacturing system including work-in-process (WIP) inventory level, utilization and throughput rate.

In this paper we provide an overall analysis of the behavior of the cycle time, WIP and utilization rates in response to changes in the fab environment using a simulation model. Moreover, various lot release patterns have been tested for their impact on cycle time distribution, WIP and utilization. From these results, the major influencing parameters and the most desirable lot release pattern could be identified. SEMATECH DATASET which has the original actual wafer fab data is used for our analysis.

In Section 2 we look at the semiconductor wafer fabrication, followed by a general description of our research approach in Section 3. The model description is in Section 4 and experimental results are discussed in Section 5. Section 6 draws the conclusion and ideas for further research.

## 2 SEMICONDUCTOR WAFER FABRICATION

Figure 1 shows the basic steps of the semiconductor manufacturing process. The overall manufacturing flow for a semiconductor firm can be divided into four stages: wafer fabrication, wafer probe, assembly or packaging and final test. One of the essential problems in controlling the semiconductor manufacturing system is to establish order release. There are a number of relevant researches on the

problem for the purpose of optimizing the production parameters including cycle time, WIP, throughput, and capacity utilization. However, as Hughes and Shott (1986) pointed out, several characteristics of the semiconductor production process have made scheduling issues particularly difficult:

(1) Reentrant Product Flows.
(2) Random Yields.
(3) Diverse Equipment Characteristics.
(4) Equipment Downtime.
(5) Shared Function of Facilities.
(6) Data availability and Maintenance.

Similar discussion can be found in Bai and Gershwin (1990), and Uzsoy et al. (1992, 1994).

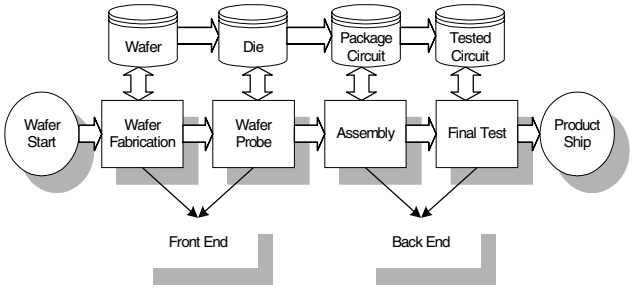


Figure 1: A Simplified Semiconductor Production Flow

Among all the processes, wafer fabrication is the most technologically sophisticated and capital-intensive phase. It is the consensus that wafer fabrication is one of the most complex manufacturing processes found today. Since wafers of pure silicon are imprinted with tens or even hundreds of patterns of an integrated circuit in layers, the sequence of processing steps in a wafer fab requires individual lots to revisit bottleneck workstations numerous times at different steps. In between such visits, a number of other workstations may be visited. For example, a wafer may have to visit the photolithography work-station eight or nine times to have all layers of circuitry fabricated. Figure 2 shows an example of the basic operations in wafer fabrication.

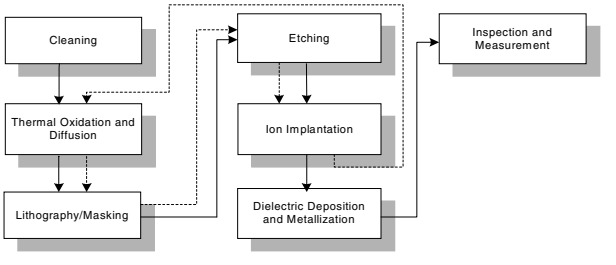


Figure 2: Basic Operation Sequence for Wafer Fabrication

In a typical wafer fab, the total number of processing steps for a wafer can easily exceed 300. Some factory processes may include a number of inspection steps. At such a step, wafers failing the inspection may be reworked.

In semiconductor industry, the total manufacturing cycle times range from 8 weeks to over 30 weeks. Stage cycle times could range from 3-15 weeks in wafer fab, 2 days to 2 weeks in wafer probe, 3 days to 3 weeks in assembly and 2 days to 4 weeks in final test (Lin 1996). Thus the wafer fabrication cycle time forms an important part of the total manufacturing cycle time.

## 3 OUR APPROACH

### 3.1 Research Objective

As mentioned in Section 2, the cycle time of wafer fabrication, 3-15 weeks, forms an important part of the total semiconductor manufacturing cycle time, 8-30 weeks. Thus it is worthy to analyze the impact of different decision variables on main production process parameters, such as cycle time, WIP, throughput, and utilization. The aim of our research is to evaluate the effects of decision variables on the cycle time, WIP, and utilization of semiconductor wafer fabrication. The selected variables are downtimes, arrival patterns, batching policy, downtime pattern and input control. For each variable, different magnitudes of their parameters would be modeled to analyze the effects on the processes. In this way, it could be evaluated which variable would be the most influential, and thus possible measures could be suggested to optimize the performance of the fab.

### 3.2 Simulation-Based Approach

Corresponding to the complexity of semiconductor manufacturing process, particularly the wafer fabrication, it is effective to use simulation to analyze and predict the dynamic behavior of the complex system. Moreover, simulation has become a popular technique for developing production schedules and dispatch lists in a manufacturing environment (Morito and Lee 1997, Mazziotti and Horne 1997). Simulation offers the advantage of developing a feasible and accurate schedule in shorter computation times compared to some of the other techniques (Mazziotti and Horne 1997, Kiran 1998).

## 4 SIMULATION MODEL

### 4.1 Model Description

We constructed a partial model of semiconductor wafer fabrication using ProModel®, a simulation software tool. The model made use of features such as machine definition, product routes and processes, machine units per hour, batch process time, and preventive maintenance schedules

as the main parameters. The data used is SEMATECH DATASET (Feigin et al. 1994).

It is assumed that all visits by all lots to a specific workstation have the same processing time distribution. And we assume that the lot size is held constant throughout the study. All machines can process only one lot at a time. Each machine is not reliable and subject to failure. Machine failures include unscheduled breakdown and scheduled maintenance. Also, we assume no yield losses in our study, although process yield may be one of the most important determinant of economic success for an IC manufacturer. Moreover, each operator is equally efficient at performing their tasks. There is no human errors made during the processing. The delays are all due to the downtimes, setup times of the machines and the resulting queues. There is only one product family being processed throughout the simulation. And the initial value of WIP in the system is zero.

In our simulation model, each lot entering the segment of the fab has a process flow that consists of 60 total operations at the 26 different stations.

Figure 3 is a flow diagram of events that would take place in the simulation model.

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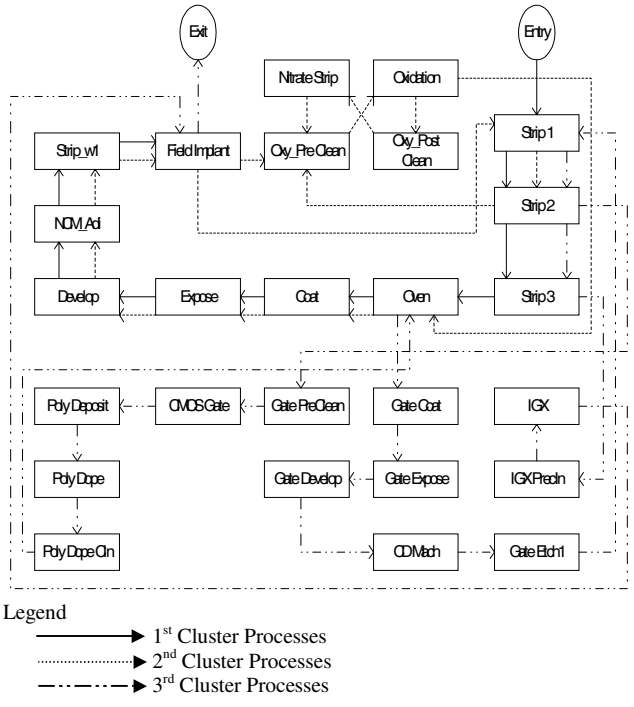


Figure 3: Flow Diagram of Processes in the Model

### 4.2 Model Verification and Validation

To verify the model, we debugged the ProModel Logic carefully and analyzed the 'trace' (Law and Kelton 1991) of the simulated cycle time of the model.

Moreover, we performed the validation by comparing the theoretical value of cycle time from the dataset and the cycle time obtained from the simulation. The theoretical value of cycle time for 1 lot as calculated from the dataset is 71.231hr, including the loading and traveling times. On the other hand, the result from simulation showed a cycle time of 71.512hr, a slight increase of 0.281hr (0.4%) which is within the tolerance set initially. From this outcome, it could be proven that the model reflects sufficiently accurately the actual cycle time of the selected processes

### 4.3 Warm-Up Period

Figure 4 shows the simulation result of cycle time for 1800 lots under N(3.65,0.5) release pattern. It is shown that the cycle time becomes more and more stable after the first 500 hours. However, it is too critical to set 500 hours as the warm-up period. Thus, we set the first 800 hours as the warm-up period in our simulation. Similar trends of stabilization could also be observed with other release distributions.

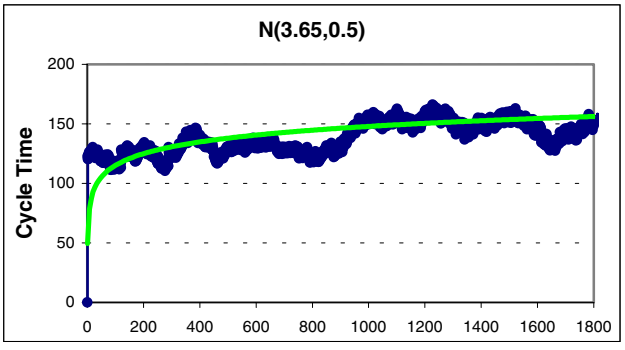


Figure 4: Average Cycle Time for 1800 Lots

## 5 EXPERIMENTATION

### 5.1 Investigation of Arrival Patterns

In this section, we will introduce the effects on cycle time and utilization by varying the pattern of the arrivals. In real life, it is difficult to control the arrival distribution demand as there are multiple external factors such as customer order schedules, transportation irregularities, etc. However, we consider a scenario whereby the fab manager could accumulate the orders and dispatch them for processing. Assume there is an order of 1500 lots of wafer. The manager has to decide on the characteristics for lot release. There are seven methods/distributions we have experimented to release them: Poisson(3.65), Poisson (4.1), Normal(3.65,0.5), Normal(3.65,2), Uniform(3.65,0.5), Uniform(3.65,2) and Random. The output behaviors for these releases were tested. Table 1 shows the results of simulation based on the FIFO dispatching rule. The results of Random arrival distribution is obviously the worst. It is reasonable since Random distribution is the most unstable

arrival pattern among them. Thus, our result analysis only focuses on the other six distributions. Figure 5 to Figure 8 descript the results of different arrival distribution except for the Random scenario.

As shown in Table 1, and Figure 5 to Figure 8, for a Poisson distribution with a mean arrival rate of 3.65 hours, there is instability in the system. There is extreme congestion in the operation with a number of equipment running close to full capacity (as shown in Table 2 and Figure 9). Under the Poisson(3.65) arrival distribution, the parameters of average value and standard deviation of both cycle time and WIP level are the worst except for that of Random scenario. Note the difference between the standard deviation of the two results using Normal distribution, although they have identical mean frequency. The one with the larger deviation produces longer cycle time and also much higher standard variation in both cycle time and WIP. This result corresponds to the theory that variability would increase the cycle time of production (Hopp and Spearman 2000, Sivakumar 2000, Sivakumar and Chong 2001). The results shown in the uniform distribution have the same trend as that of the normal distribution. The result is within expectation as there would be much variability in the arrival times of the incoming lots. The performance of Random release distribution is obviously the worst. This result has been proven mathematically (Sivakumar and Chong 2001).

Looking at the results of the seven releases, the uniform distribution would be the most preferable as it produces the best results in terms of cycle time and its variances. From the results of STD of cycle time and WIP, it is obvious that, to the standard deviation of arrival distribution, uniform distribution is not as sensitive as normal distribution. Thus for managers who want stable cycle times, the uniform distribution release pattern would be relatively desirable. Furthermore, changes in the arrival frequency would not alter its output cycle time by a significant margin, i.e. it is not as sensitive to minor changes in the arrival frequency, making it a safer policy to adopt. It is worth noting that all the release scenarios tested here are open loop patterns. It means they don't take any current system information into account. However, so far, uniform release is the most common release pattern used in actual wafer fabs due to its feasibility.

Table 1: Output Behaviors

| Arrival Distribution | Mean Cycle Time (hrs) | STD of Cycle Time | Mean WIP | STD of WIP | 95% Confidence Interval (CT) | |
|---|---|---|---|---|---|---|
| | | | | | Upper Limit | Lower Limit |
| **P(3.65)** | 135.15 | 8.52 | 34.21 | 2.64 | 158.73 | 116.22 |
| **P(4.1)** | 121.25 | 2.52 | 27.39 | 1.33 | 143.12 | 108.32 |
| **N(3.65,0.5)** | 120.98 | 2.05 | 28.07 | 1.13 | 138.26 | 109.19 |
| **N(3.65,2)** | 124.73 | 4.16 | 28.86 | 2.16 | 149.55 | 106.62 |
| **U(3.65,0.5)** | 118.53 | 0.98 | 26.25 | 1.01 | 135.78 | 104.78 |
| **U(3.65,2)** | 119.39 | 1.04 | 27.05 | 1.02 | 138.85 | 107.12 |
| **Random** | 411.41 | 68.57 | 141.51 | 24.12 | 412.90 | 388.13 |

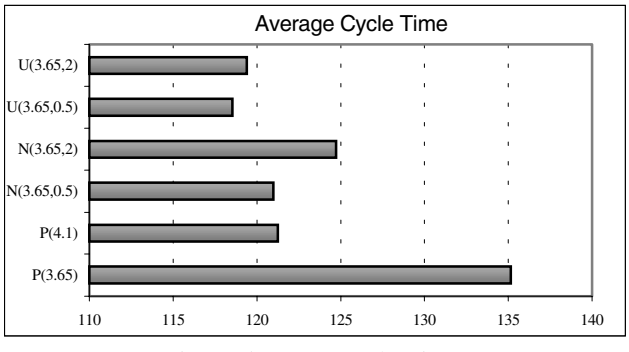


Figure 5: Mean Cycle Time

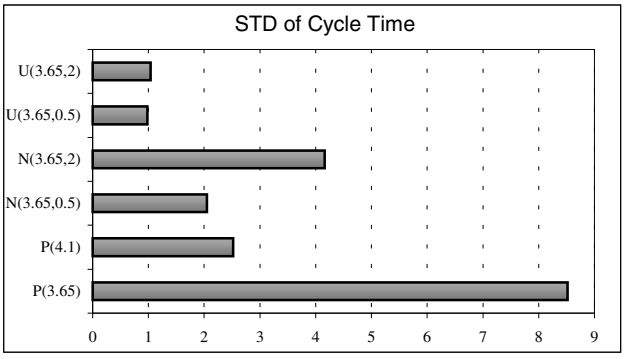


Figure 6: Standard Deviation of Cycle Time

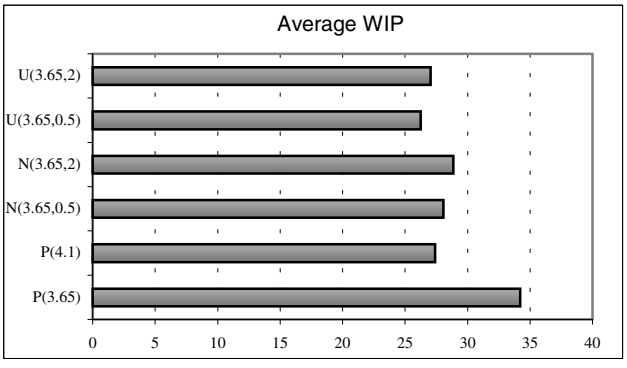


Figure 7: Average WIP

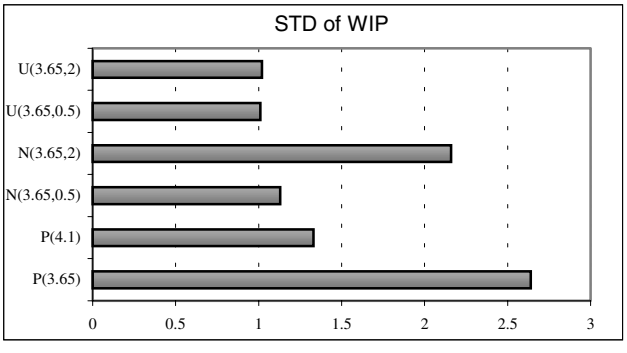


Figure 8: Standard Deviation of WIP

Table 2: Utilization of the Most Utilized Equipments

| Arrival Distribution | Oxy_PrecIn2 | Oxy_PrecIn | Leitz2 | Leitz3 | Nitrate-Strip | Oxy_PrecI1 | Develop | Strip1 |
|---|---|---|---|---|---|---|---|---|
| **P(3.65)** | 97.41 | 92.12 | 80.60 | 76.70 | 65.27 | N/A | N/A | N/A |
| **P(4.1)** | 80.42 | 79.80 | N/A | 59.80 | 58.46 | 52.22 | N/A | N/A |
| **N(3.65,0.5)** | 88.59 | 82.27 | 61.20 | N/A | 60.23 | N/A | 47.98 | N/A |
| **U(3.65,0.5)** | 81.50 | 73.69 | N/A | 62.20 | 55.21 | 49.22 | N/A | N/A |
| **Random** | 92.56 | 82.27 | 81.80 | 72.90 | N/A | N/A | N/A | 78.30 |

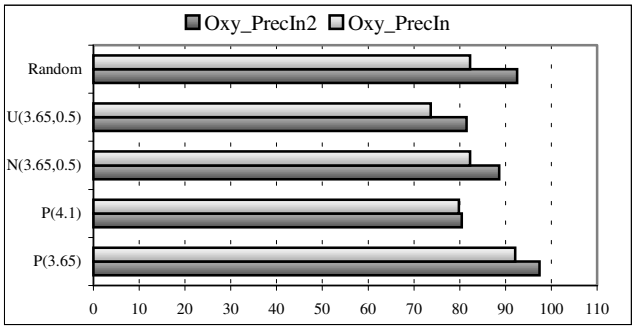


Figure 9: Two Most Utilized Equipments Under Different Arrival Distribution

In the wafer fabrication, during the warm-up period, the upstream equipment would be very busy at the start of release while the downstream ones would remain idle. Long queues would form at the first equipment. The utilization of the equipment at the upstream processes are significantly higher than that of the downstream equipment. After the system is stable, we should notice that the equipment utilization under P(3.65) and Random input distribution is much higher than that under other distribution, although other output behaviors under these two distribution are not preferable at all. It is worth noting that utilization is an important factor in choosing between these policies. Since the system has relatively high variability, higher utilization rates require much higher inventories to achieve the service level requirement (Bonvik 1996). Thus, we can conclude that the release control of the first operation has an important impact on the parameters of production process. Furthermore, lot release above the capacity constraint does not improve throughput but substantially adds to the cycle time spread (Sivakumar 2000).

### 5.2 The Impact of Batch Size

It is well known that wafer fabrication, the first portion of semiconductor manufacturing, typically involves numerous batch-processing operations, e.g. diffusion, deposition and oxidation. These operations play an important role in determining how the system performs in terms of throughput, WIP and cycle time (Fowler et al. 2002). A thorough batch size analysis would require extended study and is beyond this paper.

Table 3 shows the result of P(4.1) for 1500 lots and the result after half batch at Oxydation process. By reducing the batch size, the average cycle time for is reduced by 9.71%. However this would lead to a lower utilization of the oxidation's capacity by 18.2% (from 30.66% to 25.08%). This cycle time effect is due to a decrease in queue delay time, and it contributes to a very significant reduction in the overall cycle time.

Table 3: The Impact of Batch Size

| | Average Cycle Time (hrs) | STD of Cycle Time | Average WIP | STD of WIP | 95% Confidence Interval (CT) | |
|---|---|---|---|---|---|---|
| | | | | | Upper Limit | Lower Limit |
| **Full-Barch (base)** | 121.25 | 2.52 | 27.39 | 1.33 | 138.26 | 109.19 |
| **Half-Barch** | 109.48 | 2.40 | 24.68 | 1.26 | 129.39 | 94.74 |
| **Reduction** | 9.71% | 4.76% | 9.89% | 5.30% | 6.42% | 13.23% |

The effect of batch size on average cycle time and WIP is obvious. Furthermore, by comparing the Standard Deviation of Cycle Time and WIP, we can see that it generally adds variability into a system because items wait to form a batch and upon service completion multiple items are released to downstream operations.

### 5.3 The Impact of Downtimes Patterns

The production equipment used in semiconductor manufacturing is technologically sophisticated. It requires extensive preventive maintenance (PM) to ensure that the equipment would operate in optimum conditions. This kind of downtimes is referred to as scheduled downtimes.

In our simulation, two scenarios of this kind of scheduled downtimes were tested on the furnace (as shown in Table 4). The first one ( DT1) is that the PM is carried more frequently, but for shorter hours. The latter (DT2) is performed less often, but at the expense of longer maintenance hours, and thus higher variability.

Table 4: The Impact of Downtimes Patterns

| Scenario | Frequency (hrs) | PM Duration (hrs) | AVG for 100 lots | WIP | Utilization of Oven |
|---|---|---|---|---|---|
| **DT1** | 48 | N(6,0.5) | 135.82 | 1563 | 15.29% |
| **DT2** | 96 | N(10,1) | 137.39 | 1562 | 15.49% |

According to the simulation results listed in Table 4, the average cycle time for 100 lots for DT1 and DT2 show a 2.17% and 3.35% increment in cycle time respectively. However, the disadvantage of this arrangement is that there is a decrease of 0.2 % in the utilization of the oven by using DT1. This might be insignificant as compared to the reduction it would bring to the overall cycle time.

In actual wafer fabrication, production equipments have many unpredictable failures. It is estimated that the main cause of uncertainty in semiconductor manufacturing operations is due to unpredictable equipment downtime (Harrison 1990, Levinstein 1990). These kinds of machines breakdowns or any other impromptu circumstances (e.g. black-out) are known as unscheduled downtimes. In our future research, this issue will be considered further.

### 5.4 The Impact of Input Control

In this section, we will discuss the scenario of CONWIP. CONWIP (constant WIP) control maintains a constant work in process inventory level (Spearman, Woodruff, and Hopp 1990). According to CONWIP, when the preset WIP level is reached, no new lot is authorized for releasing into the system until a lot leaves. Figure 10 specifies the material and information flow of production line controlled by CONWIP. It can be seen as a system controlled by a single Kanban inventory control cell encompassing all machines and all part types. It combines the low inventory level of Kanban and high throughput of push system (Bonvik 1996). From a modeling perspective, a CONWIP system looks like a closed queueing network. In this paper, it is a simple representative of closed loop control mechanisms. Table 5 shows the simulation results under different WIP levels when we use CONWIP in our wafer fabrication model.

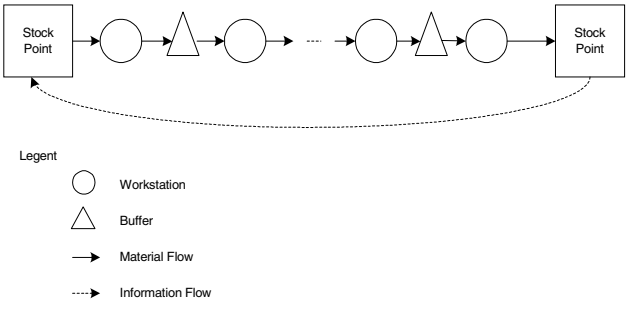


Figure 10: Basic Principle of CONWIP control

Table 5: Results of CONWIP

| WIP Level | Average CT | STD of CT | 95% Confidence Interval | |
|---|---|---|---|---|
| | | | Upper Limit | Lower Limit |
| **WIP(10)** | 121.76 | 3.84 | 183.32 | 110.27 |
| **WIP(12)** | 124.74 | 4.60 | 194.36 | 120.83 |
| **WIP(14)** | 117.77 | 1.23 | 169.16 | 112.51 |
| **WIP(16)** | 124.74 | 9.76 | 178.66 | 113.75 |
| **WIP(20)** | 122.47 | 8.98 | 161.34 | 109.33 |
| **WIP(22)** | 123.21 | 5.72 | 158.48 | 115.48 |

The results show that input control has a significant impact on wafer fabrication operations. In our simulation model, the best WIP level is WIP(14).

From Table 6, we can see that the results of CONWIP are much better than that of other arrival distributions. This results corresponds to the conclusion of Hopp and Spearman (2000), Wein (1988), and Glassey and Resende (1988). Besides the reduction of WIP and Cycle Time, it should be noticed that the key issue of CONWIP is the optimum WIP level which is closely related to the capacity constraints of bottleneck equipments in the manufacturing process. In other words, bottleneck workstations play an important role in production control.

Table 6: Results Comparison

| Scenario Percentage | WIP Level | Average Cycle Time |
|---|---|---|
| **WIP(14)** | 100(14) | 100(117.77) |
| **P(3.65)** | 244.38 | 114.76 |
| **P(4.1)** | 195.66 | 102.95 |
| **N(3.65,0.5)** | 200.48 | 102.72 |
| **N(3.65,2)** | 206.14 | 105.91 |
| **U(3.65,0.5)** | 187.51 | 100.64 |
| **U(3.65,2)** | 193.20 | 101.38 |
| **Random** | 1011.12 | 349.28 |

It is well known that the most common release control used in wafer fabrication is the open loop strategy such as uniform starts. However, any reasonable closed loop control should be better than open loop control (Glassey and Resende 1988). All the closed loop rules adjust the arrival rate to the shop so that it is negatively correlated with the queue length at the bottleneck, and the open loop rules will not consider the situations in the production process at all after the job has been released into the system.

## 6 CONCLUSIONS

In this paper we construct a simulation model of part of a semiconductor wafer fabrication using ProModel® software. The research objective is to analyze the effect of different variables in production on some selected parameters, such as mean cycle time and average WIP. The variables include job arrival distribution, batch size, downtime pattern, and input control.

The results show that the relationship between variables and system parameters are quite complex, because of the notable complexity of semiconductor wafer fabrication that includes reentrant flows, batch process, and diverse equipment characteristics.

One of the most significant conclusions from the analysis is that input control has the greatest impact on cycle time and WIP in wafer fabrication. And closed loop

system works much better than open loop system. Furthermore, lot release above the capacity constraint does not improve throughput but substantially adds to the WIP level and cycle time spread.

Our future research will focus on closed loop lot release control, considering the real time status and uncertainties in the system. Furthermore, proposed future work is to mathematically analyze the issues in complex semiconductor manufacturing processes.

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