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COMPARISON OF DISPATCHING RULES FOR SEMICONDUTOR MANUFACTURING USING LARGE FACILITY MODELS

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ABSTRACT

In this paper, we present a comparison of five dispatching rules that aim to reduce the mean and the variance of cycle times. The performance of the dispatch rules is evaluated using simulation results for two large semiconductor wafer fabrication facilities. The results show that which dispatch rule achieves the best results depends on the fab, on the load of the fab and on the product.

1 INTRODUCTION

In the era of supply chain management, the optimization of fab performance is still a hot topic in the semi-conductor business. The most common performance measures for a semiconductor fabrication facility (fab) are machine utilization, production yield, throughput, and last but not least, cycle time. We define cycle time as the time a lot of wafers needs to travel through the semiconductor wafer manufacturing process. The overall cycle time of a lot of wafers is the sum of the total times the wafer has spent in process, waiting times for all resources (such as operators, machines, tools, transportation system) needed for each processing step to become available, times elapsed during measurement and quality inspections, and the time the lot has spent in transportation.

Crucial factors of competitiveness in semi-conductor manufacturing are the ability to rapidly incorporate advanced technologies in electronic pro-ducts, ongoing improvement of manufacturing pro-cesses, and the capability of meeting due dates. In a situation where bothe prices and the state of technology have settled at a certain level, the capability of meeting due dates along with the reduction of cycle time probably has become the most decisive factor to stand the fierce competition in the global market place. Consequently, operations managers are under increasing pressure to tune the wafer manufacturing process to ensure on-time delivery. From the technical point of view, the goal of reducing processing times as well as taking care of random machine breakdowns and the unavailability of resources in general is usually reached with improved manufacturing technology that accompanies innovative physical manufacturing processes. Production logistics, on the other hand, tries to find sophisticated scheduling systems that minimize the contention for resources and consequently waiting times. However, making these decisions or designing such a system is not straightforward due to the complex manufacturing environment.

2 PROBLEM STATEMENT AND LITERATURE REVIEW

There are several factors that make production planning and control in a semiconductor chip manufacturing facility particularly difficult. For a complete summary see Hogg et. al. (1991) or Uzsoy et. al. (1992). In the following we will focus on production control and operations management as they relate to the flow of materials and the set of operations that transform raw material into the final products.

A whole spectrum of related problems have to be solved in the overall context. Depending on the technology and customer specifications, the whole manufacturing process may require up to 600 single processing steps. A typical semiconductor fab produces several products at the same time. The number of different products and material flows may approach some 200. In the past, while producing simple logic circuits, standard memory and processor chips, semiconductor fabs have been operated in a make-to-stock fashion, since production lots were usually not related to a particular order. These days, however, with ASICs and specialty processors gaining more and more market share and therefore production volume, the capability of meeting due dates has become a crucial factor in global manufacturing competitiveness.

A typical semiconductor chip manufacturing facility contains hundreds of various machines and tools such as masks used for lithography. Few machines are used for only one dedicated processing step. Most machines are designed

to carry out several very similar processing steps during the whole processing sequence and for multiple products. Machines of the same type are usually grouped into *work centers* for several reasons: Reduction of setup time, redundancy in case of breakdowns, efficient utilization of operators, and having backup when maintenance work is done.

Since the number of operations that have to be carried out exceeds the number of available machines, several of these operations are done at the same work centers. This means that a lot visits a work center more than once, in fact, up to 20 times. The process flow shows a cyclic pattern, in other words, lots of material being at different stages of processing join in front of this work center and fork after it, contending with each other for service at this work center. A manufacturing system having this feature is called a *re-entrant* line.

Furthermore, lots of wafers or single wafers may be re-routed to previous processing steps for rework if inspection detects that an operation was not done within specifications, but the wafer does not need to be discarded since it is not ultimately spoiled. These features make dispatching and scheduling particularly difficult in practice and theoretically intractable, since lots may overtake each other in a non-predictable way. The effects of overtaking on the performance metrics of queuing networks are discussed in Mittler et al. (1995).

Uzsoy et al. (1994) describe the characteristics of various approaches to the shop-floor control problem in semiconductor manufacturing. The research on this topic is reviewed and classified, and the relative advantages and disadvantages of the solution techniques used are discussed. Mittler et al. (1995) show that the efficiency of dispatching rules that utilize only local information is very limited in reducing the effects of variability on cycle times. An early study by Wein (1988) for a development and research semiconductor fabrication environment that featured only one process flow gave indication that non-local dispatching and scheduling rules significantly outperform their counterparts. Hence, in this investigation we compare a non-local dispatching and scheduling rule with two standard and two sophisticated local rules. A recent study (Rose (1999)) shows that a simple wafer fab model, incorporating essential features of a real fab, may give valuable insight in its dynamic. Naturally, of greater interest are investigations on a real fab size level, e.g. Brown et al. (1997). Unfortunately, latest research, e.g., Collins et al. (1999), Gupta et al. (1999) or Morrison et al. (1999), focus on only one advanced dispatching rule.

3 RESEARCH METHODOLOGY

3.1 Simulation Tool and Models

This investigation was conducted using the *Delphi* simulation tool as it has been available for academia until August 1995. This tool was used during the 1994 joint SEMATECH / JESSI project MIMAC („Measurement and Improvement of Manufacturing Capacity"; see Fowler and Robinson (1995)). From September 1st, 1995 on it has been distributed as ***Factory Explorer*™** (FX). This product is a package for capacity analysis of large manufacturing systems, with an emphasis on providing building blocks for modeling semiconductor manufacturing. FX combines an Excel™-based interface with two performance analysis engines – one utilizing queuing formulae and one containing a discrete event simulator.

We simulate semiconductor fabrication facilities using factory-level data sets of two different semiconductor fabs. These data sets were collected during the MIMAC project. These data sets have features as: different processes, scrap and rework, lot transportation, set-up times, batching, and machine failures. An overview of these data sets concerning the product to be manufactured, product mix, etc. is given in Table 1.

Table 1: MIMAC Data Sets #1 and #3

Data Set	Set #1	Set #3
Type of Factory	Commodity	Commodity / Logic
No. of Process Flows	2	11
Approx. WSPM	16000	21400
Avg. No. of Mask Layers	15	35
No. of Processing Steps	210 / 245	298 - 533
No. of Tools	83	73

We keep the original denotation of the data sets to avoid any misunderstandings. Each wafer type requires a certain sequence of processing steps, possibly receiving service from diverse tools. Note, that the product mix is given by the portion of one wafer type of the overall load. As a consequence, the dispatching rate of lots of wafers may differ significantly. The process flow specifications for each job type are given separately. Hence, we expect different results for every wafer type. If not mentioned explicitly, all other parameters are left unchanged.

3.2 Simulation Parameters

The fab load (lot release) defined in the original data set resulted in a bottleneck utilization of 90% for data set 1 and 70% for data set 3. In any case, statistical data was sampled only after the initial transient phase of the system. Delphi utilizes the Schruben test (Schruben (1982)) to detect initial bias in simulation output. Briefly, this test forms a test statistic that is sensitive to changes in the batch means, the method used in FX to average output and generate confidence intervals. This test statistic converges in a statistical distribution of a known characteristic against which the empirical distribution of the actual output can be tested. As a result, in both cases we sampled data of some 50000 lots. We applied the

batch means technique to calculate the confidence intervals reported in the results section.

3.3 Experimental Factors

The most sophisticated dispatch rules to reduce the mean and the variance of cycle times are

- the **Minimum Inventory Variability Scheduling** (MIVS), (see Li et al. (1996) for an introduction and Collins et al. (1999) for an application report) ,
- the **fluctuation policies for the mean of the cycle time** (FSMCT), and
- the **fluctuation policies for the variance of cycle time** (FSCVT) (both are reported in Lu et al. (1994)).

In a recent paper (Mittler and Schoemig (1999)), we showed that these rules have measurable advantages compared to standard dispatching rules when applied to small fab models. In the following, we compare these dispatch rules to the standard rules First-In First-Out (FIFO) and Earliest Due Date (EDD) using the MIMAC data sets described above.

4 RESULTS

In general, the mean (MCT) and the standard deviation (SCT) of cycle time are used to compare the different dispatch rules to each other. Apart from these performance measures, we also report 95% confidence intervals for the mean cycle time. In order to rank the dispatch rules, we calculate the start rate-weighted sum of any performance measure over all products according to the following formula:

$$x = \sum_i \frac{l_i}{l} \cdot x_i \qquad (1)$$

where l_i and x_i are the release rate and the perfor-mance measure for product i and l is the sum of all release rates.

4.1 MIMAC Data Set #1

In case of data set #1 with two products, the best performance in terms of both the mean and the standard deviation of cycle time (which are both weighted according to the product release rate) is achieved by FSVCT (see Fig. 1).

The relative improvement compared to FIFO is about 23% for the mean and 50% for the standard deviation (see Fig. 2). The cor-responding numbers for MIVS are only 5.2% and 7.5%, respectively. Due to the simpler routing, MCT and SCT as well are smaller for product 1. In terms of MCT, MIVS outperforms all other dispatch rules if we take into account product 1 only. For product 2, however, MIVS achiheves about the same results as EDD and is inferior to FSVCT. If we switch to SCT, the results of FSVCT can not be topped neither for product 1 nor for product 2.

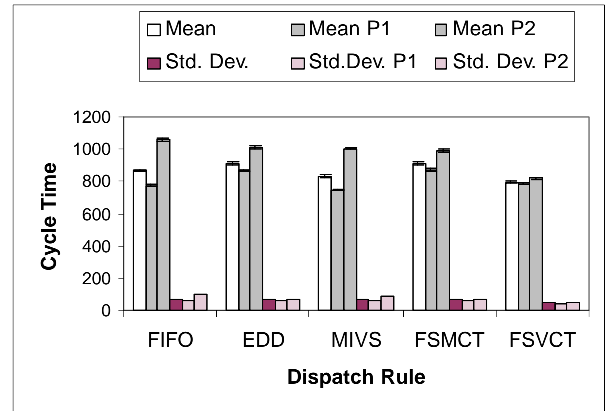

Figure 1: Mean and Standard Deviation of Cycle Time for MIMAC Data Set #1

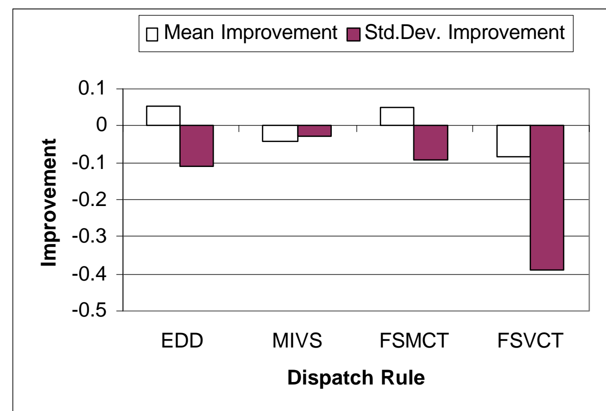

Figure 2: Relative Improvement Compared to FIFO in Terms of the Mean and Standard Deviation of CycleTime for MIMAC Data Set #1

4.2 MIMAC Data Set #3

The results for data set #3 show a completely different picture (see Figs. 3 and 4). First, the lowest MCT is achieved by MIVS. The relative improvement of MIVS compared to FIFO is, however, only about 2.5%. EDD and both fluctuation smooting policies perform worse than MIVS and FIFO as far as MCT is concerned. The relative deviation ranges from 10 to 15%. If we take into account SCT, the results of FSVCT are outperformed by any of the other dispatch rules. The relative improvement of FSVCT compared to FIFO is about 22%. MIVS performs almost the same as FIFO in terms of SCT.

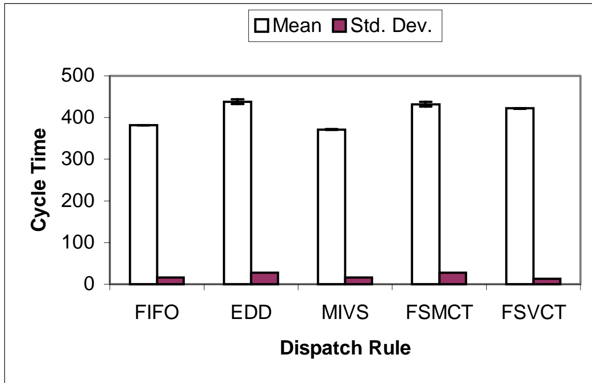

Figure 3: Mean and Standard Deviation of Cycle Time for MIMAC Data Set #3

As far as the individual products are concerned, we are not able to report due to the lack of space. However, it can be observed that there is no general ranking among the dispatch rules. The MCT and SCT results depend very much on the product and on the release rate of that product. The results, however, suggest that MIVS achieves a small product MCT if the corresponding release rate is high. Further, it is amazing that although FSVCT is devoted to the reduction of SCT, FIFO and MIVS achieve superior results for some products.

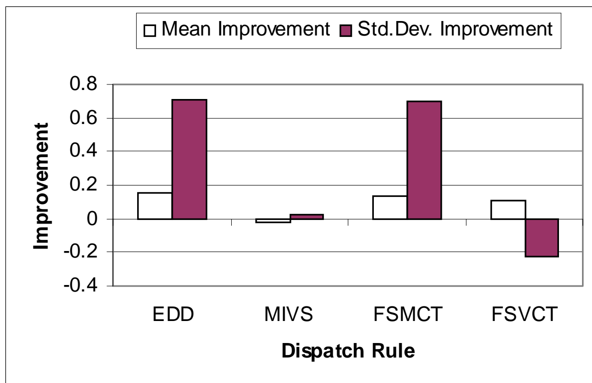

Figure 4: Relative Improvement Compared to FIFO in Terms of the Mean and Standard Deviation of Cycle Time for MIMAC Data Set #3

5 CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE RESEARCH

In this research, we have compared five dispatching rules that aim to reduce the mean and the variance of lot cycle times in semiconductor manufacturing. The major conclusion from our investigation is that findings derived for small sample models do not necessarily apply for large fabs. Obviously, the performance of dispatching rules depends on the characteristics of the fab, such as the load and product mix, the topology of the flow of material on the shop floor, and lot transportation.

Additionally, we found that in a multi-product environment a single dispatch rule could not achieve the best results in terms of the mean and the standard deviation of cycle time for all products. Due to this fact we recommend line managers use a dedicated simulation model of their particular fab for performance optimization. Academics should develop and test new dispatching and scheduling systems using several different and relatively large fab models.

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