

THE ROLE OF SIMULATION IN SEMICONDUCTOR LOGISTICS

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ABSTRACT

Concepts such as six sigma quality, continuous flow manufacturing (CFM), and computer integrated manufacturing (CIM) are critical components for success in manufacturing. However, there is much work involved in translating such concepts into competitive specific solutions that meet business objectives.

Simulation provides an effective vehicle for defining the path from competitive concepts to real world solutions. This paper presents an overview of logistics management considerations in semiconductor manufacturing and describes the critical role of simulation in the development and implementation of an effective logistics solution.

1 INTRODUCTION

Manufacturers around the world face continuing pressures to provide high-quality products with leading edge performance characteristics at competitive prices. The semiconductor industry is a prime example of this intense competition on price and performance. This competition has driven ongoing improvements in semiconductor products, producing sub-micron technologies with performance measured in nanoseconds and costs measured in millicents per bit.

State-of-the art fabricators cost hundreds of millions of dollars to build, equip and staff. New product technology costs may approach similar amounts to design, develop and qualify a technology generation. Fabricators must maximize the use of resources to achieve competitive unit costs and profitable levels of output.

Product turnaround time (TAT) or cycle time, defined as the clock or elapsed time from product release to completed fabrication, is also a critical success factor in semiconductor manufacturing. TAT has a major impact on process control capabilities, yield learning rates, product contamination

levels, product costs, and serviceability. Fabs must manage turnaround times to be successful, making TAT a key measurement in virtually every semiconductor manufacturing line.

Given the importance of both throughput and turnaround time, it is necessary to manage wafer fabrication so as to attain line throughput requirements with a minimum impact on turnaround time. In addition, manufacturing must also meet other key performance targets, including cost objectives, inventory levels, delivery commitments, process yields and labor efficiency. Concepts such as six sigma quality, continuous flow manufacturing (CFM), and computer integrated manufacturing (CIM), are recognized as important elements in managing leading edge manufacturing lines. However, it is not obvious how such concepts are translated to the specific solutions that meet manufacturing goals.

Simulation provides a quantitative methodology for defining real world solutions to complex problems. This paper focuses on the role of simulation in defining and implementing a competitive logistics system for semiconductor manufacturing.

2 MOVING, SUPPLYING AND QUARTERING THE TROOPS ...

Logistics is defined by Webster's dictionary as "the military science of moving, supplying and quartering the troops." Translated to semiconductor manufacturing, logistics is the production science of moving, processing and storing silicon wafers during fabrication.

A semiconductor logistics system includes the operating procedures to move, process and store wafers in various operational situations; the material handling solutions to physically move, process and store the wafers during fabrication; and the software control systems to logically control the execution of operating policies and material handling activities. The ultimate goal of every logistics system is to improve product flow through the line to achieve key manufacturing measurements including cost, yield, line throughput and turnaround time targets.

As Hood, Amamoto and Vandenberg (1989) described, semiconductor fabrication is a very complex manufacturing environment. It involves hundreds of advanced tools performing intricate processes one or more times on silicon wafers in a predefined flow of several hundred or more steps, with the numerous interdependences and critical parameters needed for control at each step to fabricate functional integrated circuits. Each type of equipment and individual tool has unique characteristics including process rates, batch sizes, reliability distributions, and control capabilities. Each process step has unique requirements specified in units, such as angstroms or fractions of microns, along with critical defect density, uniformity, overlay, and other specifications. Both product mix and customer demands drive set-ups and re-qualifications to process different technologies on individual tools.

The result is a very complex manufacturing environment with a high degree of variability. Variability causes many problems in manufacturing, in general, and logistics specifically, including higher rework, lower yields, larger queues, reduced throughputs and longer turnaround times. It significantly impacts the movement, processing and storage of wafers, and thus reduced variability must be an objective of every logistics solution.

A scientific approach is needed to collect the vast amounts of data associated with this complex fabrication environment, and then to systematically analyze the numerous sources of variability, the many operating constraints, and the spectrum of potential logistics solutions.

Simulation provides an effective and powerful approach for capturing and analyzing complex manufacturing systems with their associated variability and, in fact, may be the only practical production science technique available which is capable of defining an optimal logistics solution for a specific semiconductor line.

2.1 Supplying the Troops ...

A logistics solution must start with a quantitative understanding of the manufacturing line under study. One must define the product sets, process flows, available resources, production targets, and numerous other assumptions, analyzing them to quantify potential logistics solutions and predicted results. A semiconductor line model is invaluable for developing a baseline understanding of capacity, bottlenecks, and performance capability in an existing or proposed fabricator. Once a model is developed, baseline data can be generated and the performance of various operating policies for "supplying" the wafers with resources (e.g. process equipment, operators, etc.) analyzed.

For example, a production line model developed in IBM (Miller 1990) was used to simulate the key characteristics of a semiconductor manufacturing line, including process flows, equipment capabilities, equipment failures, engineering holds, rework levels, process yields, and product transport and storage. It also included manufacturing operator utilization, lot-release schemes, priority rules, batch-run sizes, lot sizes, alternate equipment options and equipment setups.

The IBM simulations provided tremendous insight into general semiconductor line performance considerations along with significant information on specific logistical policies. Key relationships between throughput and turnaround time performance were quantified, and specific recommendations were made for optimizing output versus turnaround time trade-offs.

Specifically, the simulations highlighted the importance of managing the amount of work-in-process (WIP), also known as line-loading level, in a logistics solution. WIP levels have a major effect on both TAT and throughput performance (Figure 1).

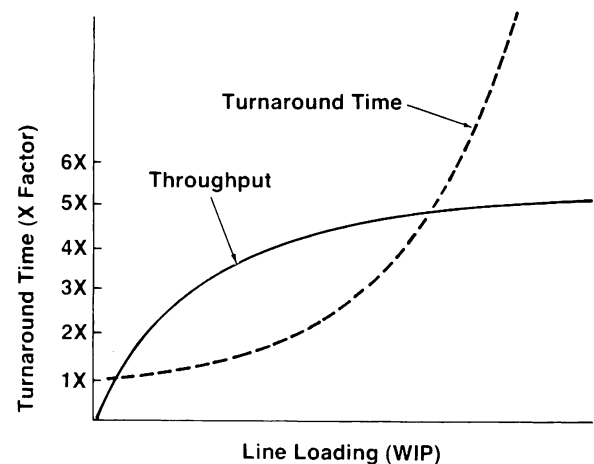


Figure 1. Effect of WIP loading on manufacturing turnaround time and throughput.

Figure 1 demonstrates the importance of line loading and the conflicts involved when attempting to improve both throughput and turnaround time. Throughput analysis techniques such as those described by Groover (1980) demonstrate that high levels of WIP increase throughput by ensuring that resources never starve for work. Throughput increases with line loading until the bottleneck capacity is saturated, and then levels off. It is intuitively obvious that the way to maximize utilization is by keeping WIP at key tools; it is much less obvious which tool(s) require WIP buffers, how large those buffers should be, or what the impact of specific buffers is on overall line performance.

Queuing theory analysis (Allen 1978) demonstrates that reduced line-loading levels provide reduced turnaround times by lowering the probability of queuing for a resource. It is important to note that throughput and turnaround time curves have inverse shapes, thereby making it impossible to optimize on both measurements. However, there are optimum WIP levels for a given throughput or turnaround time target, and it is extremely important to quantify the trade-offs between the two curves when generating throughput and turnaround time targets.

The IBM simulations lead to a 25% reduction in turnaround times in the line modeled, as a result of accurately defining the minimum WIP necessary to sustain required output volumes in the fab and then managing product releases to maintain target WIP in the line. Wein (1988) found improvements in turnaround time in the 35% to 45% range were possible by improving product release policies, while Homma et al. (1992) reported a 30% reduction in turnaround times in a Nippon Electric Corporation (NEC) fab by using simulation to define "the minimum inventory level (line loading) that is necessary to maintain a required output amount."

Line simulations further show that scheduling policies after product is released into a line generally have much less impact. Wein (1988) concluded that improvements resulting from sequencing rules were less than 10% of queuing time, while Miller (1990) also found limited benefit from global scheduling rules versus a simple first-in, first-out (FIFO) policy.

These findings strongly indicate that release policies have a major impact on line performance and must be a prime focus in any logistics management scheme, while global lot-sequencing rules and use of priority schemes should be treated as secondary considerations.

Numerous other operating policies have an effect on manufacturing performance, including alternate tool assignments, preventive maintenance schedules, staffing levels, skill levels, capacity allocations, and transport and storage procedures. There are also opportunities for applying local sequencing rules unique to specific tool(s) and operating conditions that may contribute to product flow or reduce variability in the line.

Detailed simulations allow fabs to analyze potential operating policies independently and in combination with each other to define those best for "supplying" wafers with available resources (equipment, operators, etc.). Once a fab has developed a set of well defined and effective operating policies, simulation provides the ability to continuously review and improve them as conditions change (e.g. volumes, capacity, product mix, etc.).

2.2 Moving and Quartering the Troops

Semiconductor fabrication involves several hundred process steps performed on hundreds of tools, with widely varying process times, run sizes and usage rates. Wafers must be moved, stored and retrieved hundreds of times during processing. Variability in product transport and storage is a source for potentially significant degradation in fab performance. In fact, product spends two-thirds or more of the time in a transport or storage mode in a fab running 3X or higher turnaround times.

Logistics is the science of "moving, supplying and quartering of the troops." The effective transport, storage and delivery of wafers to process tools is critical for manufacturing productivity, just as the quartering and movement of troops is critical to military success. One cannot win the competitive battles in semiconductor manufacturing if multi-million dollar tools are left idle because wafers haven't been delivered or can't be located. Pillai (1989) presents an excellent overview of the considerations and complexities involved in the design of semiconductor material handling systems in his description of material handling systems in Intel.

Product movement and storage solutions in the semiconductor industry range from totally manual approaches, where operators carry product around the fab and manually search for it when needed, to partially manual / partially automated solutions, where operators manually load process equipment but product is automatically transported and stored between process bays, to fully automated solutions where wafers are automatically delivered and loaded into tools. Most newer fabs have intelligent product stockers linked to interbay automated transport systems, and some have installed intrabay automation; while older fabs tend to use manual product transport and wire racks for storing product.

Simulation models are widely used to quantify the trade-offs between viable material transport and storage options. In general, they show that manual solutions are more variable and/or have higher operating costs because they are labor intensive, while automated solutions require higher initial capital investment for the automation hardware and software. The quantifiable benefits associated with automated material handling systems are attributable to reductions in variability that translate into such measurements as increased resource utilization, higher throughput and reduced turnaround times.

IBM has used material handling simulations to analyze potential material transport and storage sys-

tems. The models include definition of product storage points (locations, capacities, access times, etc.) and transport systems (method of transport, paths and distances, speeds, intersections, etc.), and predict the results of various alternatives. Analysis in one fab predicted improvements in turnaround times from 6% to 33%, and increases in throughput from 4% to 24%, depending on the extent of the automation (limited interbay to full intrabay) versus manual material handling solutions.

The reduction in variability associated with material handling automation shifts the throughput and turnaround time curves in Figure 1 (Figure 2). Other published results describe performance improvements associated with automated material handling systems similar to those modeled in IBM. Many describe additional benefits in areas like labor productivity, process yields, and final test yield performance (Holton et al. 1988, for example).

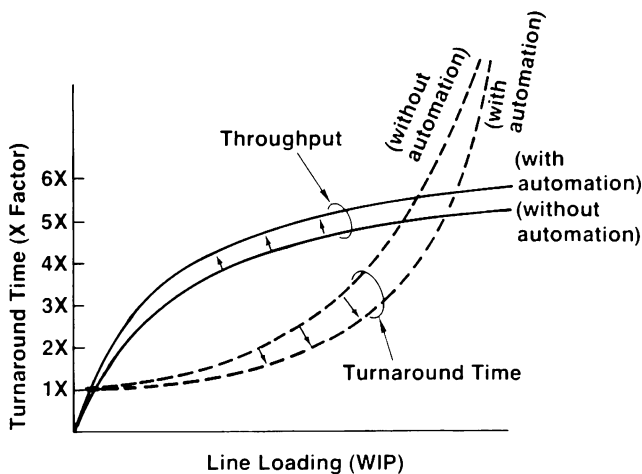


Figure 2. Effect of automation on turnaround time and throughput curves.

While there is little debate concerning the ability of automation to improve manufacturing performance, there remains significant debate in the industry concerning the optimum levels of automated material handling in semiconductor manufacturing. The issues include the capital cost of automated solutions versus the operating costs associated with human solutions, and the subsequent effect on manufacturing measurements. While there is a wealth of analysis on release and scheduling policies in the literature (Uzsoy Lee and Martin-Vega 1990, for example), there is surprisingly little comparing automated versus manual systems for moving and storing product.

Regardless of whether people or automated systems are used to move and store product, simulation should play a key role in the evaluation and design of wafer transport and storage logistics. The design and execution of logistical solutions to move and store wafers is a complex problem with significant implications on product flows and operational variability, and fabs require a set of well-defined and effective operating procedures to succeed.

2.3 Logistics Control Software

Most fabricators find it very difficult to approach 80% utilization of their expensive production resources or to approach turnaround times below 2X RPT. Clearly, an opportunity exists for improving manufacturing performance in most fabs, with significant financial benefits resulting. The traditional concept of a semiconductor logistics system which tracks product status must be replaced with an integrated logistics solution built on well-defined and validated operating policies, effective and predictable material movement and storage solutions, and logistics control software designed to support product flow and reduce variability (Miller and Anastasio 1991). Figure 3 depicts the primary components of an integrated logistics solution.

Today's logistic software systems generally include an online, real-time product tracking capability, with interfaces for updating status either manually or automatically. Most documentation is maintained in electronic form, and links may exist to process equipment to automatically load recipes and collect process results.

While such tracking and control could theoretically be done manually, in practice every fab has invested significant amounts in computerized logistic software systems, indicating that the complexity of the environment dictates the use of computerized tracking systems.

Logistics software must continue to evolve from the promise of today's research to the reality of providing enterprise-wide logistics control. It must incorporate more functionality to encode and enforce critical operating policies, and execute control decisions where feasible, including automated product movement and storage, adaptive process control to compensate for equipment and process variability, and advanced logistics control capabilities such as expert systems or short-interval-schedulers, to react to unplanned events.

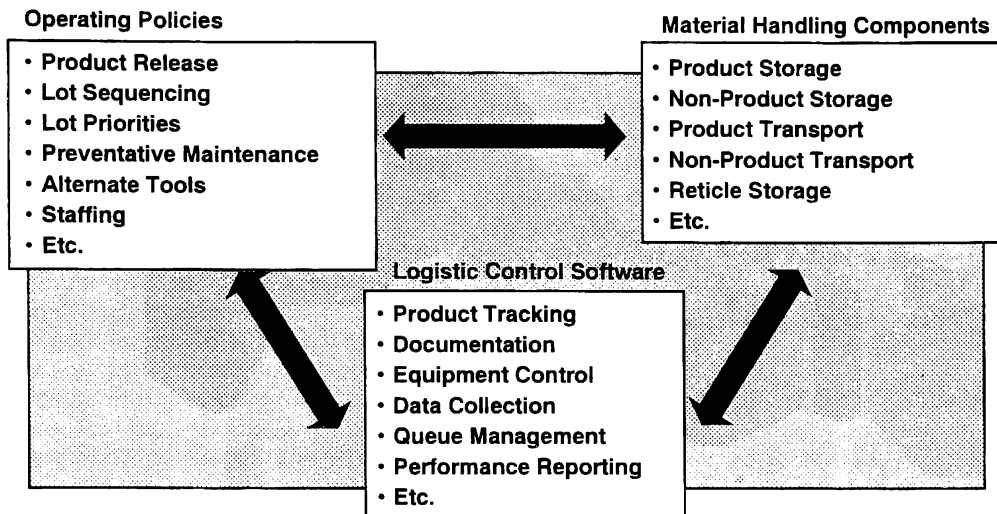


Figure 3. Interrelationship of an integrated logistics solution.

3 DISCUSSION

Semiconductor logistics is the production science of managing the movement, processing and storage of wafers in such a way as to achieve key manufacturing objectives. The primary focus of every semiconductor logistics system must be to improve product flow and reduce variability. A logistics solution has a significant impact on the performance of the fabricator and, thus, on the profitability of the firm. As seen above, improvements in release policies, material handling and other key logistical decisions may provide significant improvements on critical manufacturing measurements.

Semiconductor fabrication is a very complex manufacturing environment. The definition and implementation of a logistics management system requires a powerful analysis technique to develop an integrated solution of well-defined operating policies, effective material transport and storage components, and functional control software.

3.1 Is Simulation Necessary?

Simulation requires skilled personnel, dedicated time, and sophisticated resources to develop, validate and apply accurate models. This is true in every simulation area, from chip design and process simulations to yield model and production line simulations. This fact leads many people to use less costly, more straight-forward techniques including spreadsheets and deterministic models. The question is, do these simpler analysis methods provide fabricators with sufficient information to make optimum logistical decisions about such things as equipment purchases, line layouts, operating policy definitions, staffing levels, etc.

Hood (1990) and Baudin et al. (1992) reviewed the need for detailed simulation models versus spreadsheets or simplified models, and both found simulation is required to produce accurate results. Key performance measures, including resource utilization, WIP levels and turnaround times, varied by more than 20% from actual levels in Hood's analysis when the models ignored such factors as equipment reliability or operator staffing. Baudin found that spreadsheet analysis lead to overstatement of capacity and, thus, a lack of key resources including equipment and space.

The reasons for these findings are that variable or stochastic behavior is a major component in semiconductor manufacturing and cannot be ignored without potentially seriously compromising analysis results; and that semiconductor manufacturing is extremely complex and that this complexity must be analyzed and understood in order to make competitive logistical decisions.

3.2 Focus on Variability

Variability is the "enemy" of every manufacturing line and logistics system, affecting every operational plan, policy and measurement. If one could completely eliminate variability in a fab and provide a balanced capacity across the equipment set, then 100% utilization of resources at 1X product turnaround times could theoretically be achieved.

This is not possible today for many reasons, starting with the physical processes and equipment sets themselves. Technical requirements and equipment economics drive differences in batch sizes and process times, which introduce variability independent of any "uncontrollable" events.

As an example of this "built-in" variability, take a simple two-step process. Step 1 is a four-hour operation in a tool capable of processing 100 wafers per run, while step 2 is a one-hour process in a tool running 25 wafers at a time. Assume 100% equipment and operator availability, no transport time, and 100 wafers arriving at step 1 every four hours. Even in this perfect manufacturing world, only the first 25 wafers can be processed at 1X RPT. The other wafers must queue at the second tool. As a result, the average TAT will equal 1.3X RPT for both steps at 100% utilization.

Equipment reliability and process capability are major sources of "uncontrollable" variability. Variability in arrival rates, service times and availability distributions can have a significant effect on manufacturing performance at a single process step (Martin 1993). The analysis becomes extremely complex over hundreds of steps on hundreds of machines with unique reliability assumptions, re-entrant flows, rework probability, and alternate tool options. Line simulation models are needed to examine the effect of preventive maintenance schedules, backup tool assignments, local sequencing rules, etc. on line performance measures.

People are a major source of variability in manufacturing. One of their key strengths is flexibility, however, variability is also one of their major weaknesses. Flexibility is critical in many manufacturing tasks (e.g. problem determination and resolution) so there will always be a need for skilled personnel in semiconductor manufacturing. However, repeatability is critical in many other tasks (e.g. product handling and equipment loading) so it is important to analyze whether human or automated solutions are better for executing a specific task.

The issue of human flexibility versus variability is very complex, and has many implications for fab performance and logistic system designs. The analysis of variability caused by people in a fab is an area ripe for additional research and simulation. While there has been some work on staffing levels vs. fab performance, much needs to be done to quantify the implications of automation vs. staffing and skill levels in fabs to reduce the level of manufacturing variability.

4 SUMMARY

The effort required to develop and maintain accurate production line simulation models must not be underestimated. Neither should the competitive edge provided by high leverage logistic solutions based on detailed quantitative analysis.

The use of simulation to analyze, define and implement logistic solutions provides significant leverage in semiconductor manufacturing performance. While this paper has referred to just a couple of examples, there are literally hundreds of specific cases published in the semiconductor industry (see Fowler and Robinson 1994, for example).

Most companies have strong motivation and significant opportunity to improve fabricator performance. Given the wealth of data that demonstrates the benefits of simulation in defining and implementing effective manufacturing solutions, it is surprising that many fabs still rely on deterministic techniques to make major decisions in areas ranging from equipment purchases to staffing plans. It is even more surprising how many logistical decisions, such as layouts, operating policies and material handling solutions, are based on human judgement or other subjective criteria.

Much opportunity remains for improving semiconductor manufacturing performance via the application of simulation analysis. The complexity and variability inherent in a wafer fabricator demands the use of stochastic simulations to define the competitive solutions necessary, for success today and into the future.

5 CONCLUSION

Semiconductor manufacturers require robust logistics capabilities to move, process and store wafers during fabrication. The massive financial investments and intense competition demand a logistic solution that supports high manufacturing productivity at competitive costs.

The complexity of the semiconductor manufacturing environment makes it especially difficult to analyze and define an effective logistics solution. Concepts and philosophies are nice, but detailed analysis based on production line simulation is critical for success.

It would be inconceivable in most semiconductor companies to design and develop a new technology without the significant application of simulation models to define and verify product designs and processes. The same level of quantitative analysis is required in the design and implementation of logistics management solutions, given the performance implications of a sub-optimal logistics solution on fab investments that are approaching one billion dollars.

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REFERENCES

- Allen, A. O. 1978. *Probability, statistics and queueing theory*. New York: Academic Press.
- Baudin, M., V. Mehrotra, B. Tillis, D. Yeaman, and R. A. Hughes. 1992. From spreadsheets to simulations: a comparison of analysis methods for IC Manufacturing Performance. In *Proceedings of the 4th Annual International Semiconductor Manufacturing Science Symposium*, Institute of Electrical and Electronics Engineers, Piscataway, New Jersey.
- Fowler, J. and J. Robinson. 1994. Measurement and improvement of manufacturing capacity (MIMAC) project bibliography. SEMATECH, Austin, Texas.
- Groover, M. A. 1980. *Automation, production systems, and computer aided manufacturing*. Englewood Cliffs, New Jersey: Prentice-Hall.
- Holton, W. C., J. Dussault, D. A. Hodges, C. L. Liu, J. D. Plummer, D.E. Thomas, and B. F. Wu. 1988. Computer integrated manufacturing (CIM) and computer assisted design (CAD) for the semiconductor industry in Japan. Department of Commerce Japanese Technology Evaluation Program Panel Report.
- Homma, W., N. Miyatake, Y. Miyajima, I. Kikuchi, S. Tohnai, J. Ueno, T. Torii, M. Enomoto, N. Minami, M. Fuyuki, and I. Inoue. 1992. Line productivity improvement using simulation system for VLSI manufacturing. In *Proceedings of the Fall Meeting of the Electrochemical Society*, 13-17. Electrochemical Society, Pennington, New Jersey.
- Hood, S.J., A. E. Amamoto, and A. T. Vandenberg, 1989. A modular structure for a highly detailed model of semiconductor manufacturing. In *Proceedings of the 1989 Winter Simulation Conference*, ed. E.A. MacNair, K. J. Mussalmen and P. Heidelberger, 811-817. Institute of Electrical and Electronics Engineers, Piscataway, New Jersey.
- Hood, S. J. 1990. Detail versus simplifying assumptions for simulating semiconductor manufacturing lines. In *Proceedings of the Ninth IEEE International Electronics Manufacturing Technology Conference*, 103-108. Institute of Electrical and Electronics Engineers, Piscataway, New Jersey.
- Martin, D. P. 1993. Key factors in designing a manufacturing line to maximize tool utilization and minimize turnaround time. In *Proceedings of the 5th Annual International Semiconductor Manufacturing Science Symposium*, 48-53, Institute of Electrical and Electronics Engineers, New York, New York.
- Miller, D. J. 1990. Simulation of a semiconductor manufacturing line. *Communications of the ACM* 33:98-108.
- Miller, D. J. and F. J. Anastasio. 1991. World class manufacturing: sink or CIM. In *Advanced Semiconductor Manufacturing Conference Proceedings*, 32-38. Institute of Electrical and Electronics Engineers, Piscataway, New Jersey.
- Pillai, D. 1989. Designing automated material handling systems for large-scale wafer fabrication automation. In *Proceedings of the Semiconductor Manufacturing Conference*, MS89-785. Society of Manufacturing Engineers, Dearborn, Michigan.
- Uzsoy, R., C-Y Lee L. A. and Martin-Vega. 1990. A review of production planning and scheduling models in the semiconductor industry. Research Memorandum 90-11, Department of Industrial Engineering, Purdue University, West Lafayette, Indiana.
- Webster's new world compact school and office dictionary. 1982. New York: Simon and Schuster.
- Wein, L. M. 1988. Scheduling semiconductor wafer fabrication. *IEEE Transactions on Semiconductor Manufacturing* Vol. No. 3:115-130.

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