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RAPID MODELING: IN THE DESIGN OF A NEW PCB MANUFACTURING SYSTEM

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ABSTRACT

The ability to quickly model the production implications of changes from marketing, sales, finance, or engineering allows manufacturing enterprises to be pro-active in building competitive advantage. The power of a rapid modeling approach that assists manufacturing system designers and planners to evaluate their factory production systems is illustrated here. The study demonstrates how various members of an interdiciplinary design and analysis team can evaluate the process capabilities before introducing new methods and machines.

I. INTRODUCTION

The process by which products are coming to market is becoming shorter and causes a need for more integration of different functions of the business enterprise. The existence of design tools that can reliably evaluate the unsoliticitous changes in product mix on system lead time and resource utilization is useful during both the design phase and operational phases of the manufacturing system life cycle. Different departments make different decisions that all impact the system design and costs; these same departments often use different decision support tools that sometimes cause inconsistent conclusions and thus cause the manufacturing managers to pursue less than optimal strategies. Most current planning tools such as MRP, CAD/CAM and CAPP are not useful in the design of a manufacturing system. These tools suffer one or more inherent problems when used for purposes they were not designed for, such as "being after the fact", being bookkeeping oriented and most importantly being static where the systems are dynamically changing. We use a case study to illustrate the power of approaching a manufacturing system design problem from the prospective of the industrial, test, and quality engineers working on the interdisciplinary design team. The cohesion for this team is decision support tools that force them to study the impact of their decisions on the rest of the design and communicate the interdependencies of all their decisions.

II. ATTRIBUTES OF RAPID MODELING TOOLS

The desirable attributes of rapid modeling tools for manufacturing systems modeling and evaluation include the following. A necessary requirement for the software this team used was being able to quickly model and analyze the effects of their decisions. Modeling and evaluating manufacturing systems is advantageous because a dry run and fine tuning of such systems can be done inexpensively on the computer before undertaking the "real thing" which is expensive. Rapid modeling techniques appear to come the closest to serving this need.

Analysis after all the pieces have been built is much easier but does not help one consider many alternatives before committing resources. As manufacturers change the manufacturing process, it is expected that the costs and cost structures will change as well [11]. For example, if lead time is to be reduced in an electronic assembly facility, replacing manual equipment with faster automated equipment might lead to a requirement for additional printed circuit board burn-in capacity. The subsequent changes in volumes and product mixes may also be an important part of the the requirements for a new manufacturing system. These factors are an integral part of the justification process and should be included in the model as well.

We expect a good rapid modeling tool to effectively model and evaluate the implications of alternative resources and processes on such performance measures as

production capacity, machine utilization, queues, work-in-process inventory and leadtime. Equally important, it should allow, indeed encourge, the design team to ask what-if questions frequently, and that they expect answers swiftly and painlessly, without programming or other special computer expertise.

A further desirable attribute is the ability to communicate with other software tools that may already be in use at the manufacturing enterprise. For instance, the engineering parameters dealt with by rapid modeling should be easily exportable to a cost analysis program that looks at profit implications of changes in the manufacturing process.

III. CASE STUDY: DESIGNING PCB TEST LINE

The *PlutoX* project cited below, is based on a study of a manufacturing system that contains complex printed circuit boards containing ASICS. Implications of changing volumes and product mixes on product lead times will be shown from both the Industrial and Quality Engineering perspective.

The design team objectives are to develop a successful test strategy that arranges the various testers in the circuit board manufacturing process in a way that will result in products of maximum quality and reliability at minimum cost.

1. The Design Problem -- A Scenario

PlutoX is scheduled for market introduction in 1991, and is to be produced in the *DOGBOARD* factory. This new design will use a 16-bit microprocessors and other application specific VLSI circuits. The *Marketing Department* has specified extremely compact packaging so that the product can fit on the desk of the receptionist in small companies and professional offices. To fulfill this requirement, the engineers have decided to use surface mount technology(SMT) on double-sided printed circuit boards.

Everyone at *DOGBOARD* expects the new product to be a success. The company is committed to building a new automatic PCB assembly cell, not only for added capacity, but because boards using surface mount technology and VLSI cannot be built and tested using the present manufacturing line. The *manager of test engineering* has been assigned the task of devising a production test strategy and the test equipment recommendations for *PlutoX*. Senior Management (Plant, Manufacturing, Finance) have asked for an estimate of acquisition and operating cost as well as the projected return on investment. Management is aware of the $1 million per tester price tag for the equipment to test *PlutoX*. They have also requested a manufacturing plan that will allow them to use the lastest industry practices including *lot size one - entity processing, JIT, minimum product testing cost, etc.* for modernization of the test facilities to accommodate future products by their modernized assembly cell.

The recommendations are to be formulated and made to senior management in one month. These recommendations should be analyzed using modeling and simulation tools that will be useful during the planning, analysis, design, and operation of the proposed system. The test manager has some insight into a set of modeling tools used for the design of the custom integrated circuits used in *PlutoX*. The engineering department was able to use a workstation based design methods that allowed them to design and commit to silicon their designs in less time without errors. The methods used allowed them to develop both the design and the test methods concurrently and will allow them to begin the manufacturing phase in less than one year. The manufacturing team decided to use a design workstation with modeling and simulation tools comparable to that used in the design of *PlutoX*. The design workstation for *PlutoX* integrated register transfer level, logic and fault level, and circuit level modeling and simulation tools with a graphic schematic capture system. The test engineer suggest that the manufacturing design team use the rapid modeling tool set describe in a recent paper he read on computer aided design [3]. This tool set uses MANUPLAN, a tool similiar to a register transfer level hardware description language used for ASIC design, and SIMAN, a discrete event simulation (DES) language similiar to a logic and fault simulation language used in ASIC design and test. SIMSTARTER a DES model generator that connects MANUPLAN and SIMAN.

2. Variables that affect the Design

An estimate of the technical variables that will affect the test strategy are:

- Forecasted production rate = 200 - 500 boards/week.
- *PlutoX* will consist of 3 boards, all to be produced in equal quantity. In terms of function, density and size, the PCBs will be significantly different from the the designs currently made by DOGBOARD.
- Component and Process Quality --The process average is 50-70%.

- The maximum flowtime including a 72 hour dynamic burn-in for two of the three PCB's , through the test cell shall not exceed five days.

PlutoX is now in the planning phase, but because of the current factory problems, the Manufacturing Engineering Department is not able to determine completely the future facility needs. The Manager of Product Assurance has been asked to carry out the new corporate Q95 policy on *PlutoX*; this policy requires a 95% yield at each process step. The yield has been found to be an important parameter in determining the investment cost for future resources and the test strategy. Achieving 95% yield at each process step implies a significant cost savings in test resources. The *Quality Manager* has recently set up a manual entry data collection system to monitor and verify the process yield. To date, this system has been useful in substantiating what is already common knowledge about the parts and process problems for current Work in process (WIP). A reliable estimator for the yield will require six more months of data collection and analysis. In the meantime, both managers have assumed a start up yield of 50% for *PlutoX*, they predict that as the product matures, the use of VLSI and SMT will ultimately result in a reliability and yield improvement that will achieve the Q95 level.

The *Test Manager* also knows that *PlutoX* design complexity will cause more operational defects during the start-up phase, and that the support from the Engineering Department will have to be increased if DOGBOARD is to deliver the 100 demonstration units on time. The current manufacturing experience on systems produced shows that they can expect many design and component part problems that usually results from design flaws. Many of complex devices and the reflow solder process used for SMT could cause intermittent failures on the PCBs. These might escape the first level in-circuit test and the nummerous defects that might not be detected is not known for SMTs. In order to maintain a five day flow time, extra test and repair capacity must be planned for. To verify a working design before making recommendations to Senior Management, the design team has decided to include in the analysis the impact of various lot sizes on test resources.

IV. ANALYSIS RESULTS AND RECOMMENDATIONS

Using MANUPLAN, SIMSTARTER, and SIMAN, the manufacturing design team provided their recommendations to Senior Management. The modeling and simulation tools allowed them to analyze many alternatives and to decide on the following optimized design. This design meets most of the objectives and constraints as defined.

1. Test Equipment Requirements for *PlutoX*

Because the large setup time to test time ratio, for each PCB, the lot size one policy was not attempted.

The test line is capable of providing the flow time of 5.3 days at the 500 PCB/week production rate by using overtime.

The configuration and tester resources needed are illustrated in Appendix Table 1 below.

The values for utilization and flowtime for each resource for the various production levels are shown in Appendix Table 2 below.

2. Use of Simulation to Size the Burn-in Resource

The 72 hour burn-in requires a system for dynamically operating the PCB's at an elevated temperature. These storage facilities are expensive and simulation is useful in determining the capacity and size of this resource. Simulation was also useed in determining the optimal sizes of all the buffers/storage areas. The effects of maintenance and repair policies on the system throughput were studied.

3. Impact of Lot Size on Test Resources

Table 1 Shows the changes in utilization for Lot size. Based on these data, the team concluded that the investment in equipment to run lot size of less than four was not cost effective unless the setup times could be significantly reduced. The team recommended that the increasing the lot size as the production rate increased would maximize the utilization of the resources. The penalty paid would only be in the increase in flow time. The 5 day (in reality 1 week) flow time requirement would be slightly exceeded as shown in Appendix TABLE 3 below.

The flow time decrease is because of the overtime. Pieces that are completed on overtime appear to have 0 flow time during the regular 2 shift day. Note that the increase in flow time for lot size of 4 to 10 is greater than that for lot size of 10 to 12. The lot size is a significant factor in the resultant product flow time. [2]

4. Impact of Start-up on Test Cell Performance

During the production start up phase, the cell has excess capacity for debugging the product and the

manufacturing process. The analysis shows that the resource utilization, except for ICT, is less that 80%. There is also an additional shift available for overflow.

V. CONCLUSIONS

The interdisciplinary team used these initial designs as starting points for further analysis. The major benefits of this method is that it clearly defines the tradeoffs that are necessary and the important issues that need to be studied further.

During the planning and specification phase of the project, MANUPLAN [14] was used to explore the numerous alternatives and to optimize the system. Once optimized, SIMSTARTER [15] was used to create the SIMAN [17] modeling language, model (.mod) and experiment (.exp) files. SIMAN was used to determine the size of the burn-in facility and the maximum sizes of all storage areas and material handling constraints. The design workstation hardware used by the interdisciplinary design team with each team member analyzing the design from the finance, quality, configuration and marketing perspectives consisted of Apollo with the UNIX operating system and IBM AT with DOS 3.3.

A rapid prototyping method that is similar to that used for designing application specific integrated circuits (ASICS) was used to design the test and inspection line for *PlutoX*. The tools used are linked together in a way that allows them to be used from a common interface for marketing, finance, manufacturing and quality personnel [1]. Thus the advantage gained by using workstation based modeling and simulation tools for designing manufacturing systems is equivalent in importance and power to the advantages gained from tools for inserting the VLSI silicon technology into the new products. Both technologies enhance the competitive advantage of the business enterprises using these methods.

The planning and design method shown, allows the enterprise to leverage their expertise in design, manufacturing, quality, marketing and finance in a cooperative and productive manner. The entire enterprise, not just one department, can optimize the tradeoffs among the choices in order to deliver high quality products in a timely and cost efficient way.

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Table VI-1: *PlutoX* Test Cell Configuration

Equipment Name	No. in Group
In-Circuit Testers (ICT)	4
Function Testers (FNT)	2
PRE-Burnin (PREB)	2
Burn In Slots (BI)	660
Level 2 Test (LEV2)	5
Inspection (INSP)	4
Repair Stations	1
System Integration (MATCH)	4

Table VI-2: System Utilization and Flowtime

PRODUCTION RATE	200/week	400/week	500/week
Lot Size	4	10	12
Days worked	5	6	6
Shifts per day	2	2	2
OVERTIME	None	None	(Range from None

Equipment Name	Number Needed	Utilization(%)		(Overtime)	Overtime
ICT	4	61.8	84.4	85.7	(20%)
FNT	2	46.7	57.8	69.4	(0%)
PREB	2	59.1	78.8	79.8	(20%)
BI	660 slots	60.8 (Sat)	84.0	84.1	(1 Shift)
LEV2	5	31.0	34.4	33.5	(1 Shift)
INSP	4	50.5	81.2	80.4	(1 Shift)
REPR	1	*	*	*	
MATCH	4	17.2	17.7	22.1	(0%)

* Repair utilization was not measured
(Sat) means Saturday was worked on this equipment
(1 Shift) means a complete 3rd shift was worked

```
 ---- network dynamics, inc. ---- manuplan program input (v.1.1) ----
                  run title:  PlutoX--400 Boards/Week--WSC89
 version  : II/1.1
                  ---- results from manuplan follow ----
                        **** production summary ****
    the desired production can be achieved, with
    resulting w.i.p. and system flow times as below
  part no.      annual production    flow time (days)    w.i.p. (pieces)
                  good   scrap
  PCB149         400.00    .000         5.0103            334.02
  PCB259         400.00    .000         .69834            46.556
  PCB369         400.00    .000         5.2238            348.25
  PCB            400.00    .000         .10673            7.1155
                                  total w.i.p. (pieces) =  735.94

                  **** equipment utilization summary****
equipment   no. in       --utilization (%)--            w.i.p.(no. lots)
  group     group     setup    run  repair  total   in process waiting  total
ICT           4      12.2    70.9    1.25    84.4    3.33     1.14       4.46
```

Table VI-3: Impact of Lot Size on Flow time

PRODUCTION RATE	200/week	400/week	500/week
Lot Size	4	10	12
Days worked/week	5	6	6
Shifts per day	2	2	2
OVERTIME	None	None	(Range from None to Full shift)

Equipment Name	Number Needed	Time Spent at Station (Overtime)			
				Overtime	
ICT	4	136 min	323.8	322.0	(20%)
FNT	2	55	109.0	147.6	(0%)
PREB	2	89.1	239.8	238.0	(20%)
BI	660	4800 (Sat)	4800	4800.0	(1 shift)
LEV2	5	91.6	160.0	150.1	(1 shift)
INSP	4	99.9	210.4	228.7	(1 shift)
REPR	1	40	102.1	123.4	
MATCH	4	66.0	102.4.	102.8	(0%)
Max ICT-MATCH(Days)		5.4 days	6.2 days	4.4 days	
		1.12 weeks	1.05 weeks	0.75 weeks	

* Repair utilization was not measured
(Sat) means Saturday was worked on this equipment
(1 Shift) means a complete 3rd shift was worked

Table VI-4: Input/Output Data for *PlutoX*

FNT	2	12.5	41.7	3.61	57.8	1.08	.431	1.51
PREB	2	12.5	62.5	3.75	78.8	1.50	1.39	2.89
BI	660	7.58	.000	.842	8.42	50.0	5.56	55.6
LEV2	5	5.56	27.8	1.11	34.4	1.67	.772E-01	1.74
INSP	4	4.30	76.1	.804	81.2	3.21	1.40	4.61
REPR	-1	.000	.000	.000	.000	2.10	.000	2.10
MATCH	4	7.29	10.4	*********	17.7	.708	.322E-02	.712

details for individual parts

PCB149	operation	equipment	wip	flow time (mins)	time per visit
	LEVA	ICT	8.5355	122.91	122.91
	LEVB	FNT	7.5701	109.01	109.01
	PREB	PREB	12.255	176.48	176.48
	BURN	BI	277.78	4000.0	4000.0
	LEV2	LEV2	6.3273	91.113	68.335
	INSP	INSP	14.609	210.37	157.78
	REPR	REPR	6.9444	100.00	150.00

from operation	to operation	for each piece of good prodn: no. of pieces that are routed through this branch
DOCK	LEVA	1.0000
LEVA	LEVB	1.0000
LEVB	PREB	1.0000
PREB	BURN	1.0000
BURN	LEV2	1.0000
LEV2	INSP	1.3333
INSP	STOK	.66667
INSP	REPR	.66667

REPR	LEV2	.33333
REPR	STOK	.33333

PCB259	operation	equipment	wip	flow time (mins)	time per visit
	LEVA	ICT	22.483	323.75	283.28
	INSP	INSP	16.931	243.80	213.33
	REPR	REPR	7.1429	102.86	180.00

from operation	to operation	for each piece of good prodn: no. of pieces that are routed through this branch
DOCK	LEVA	1.0000
LEVA	INSP	1.1429
INSP	STOK	.57143
INSP	REPR	.57143
REPR	LEVA	.14286
REPR	STOK	.42857

PCB369	operation	equipment	wip	flow time (mins)	time per visit
	LEVA	ICT	13.610	195.99	195.99
	LEVB	FNT	7.5701	109.01	109.01
	PREB	PREB	16.630	239.48	239.48
	BURN	BI	277.78	4000.0	4000.0
	LEV2	LEV2	11.111	160.00	120.00
	INSP	INSP	14.609	210.37	157.78
	REPR	REPR	6.9444	100.00	150.00

from operation	to operation	for each piece of good prodn: no. of pieces that are routed through this branch
DOCK	LEVA	1.0000
LEVA	LEVB	1.0000
LEVB	PREB	1.0000
PREB	BURN	1.0000
BURN	LEV2	1.0000
LEV2	INSP	1.3333
INSP	STOK	.66667
INSP	REPR	.66667
REPR	LEV2	.33333
REPR	STOK	.33333

PCB	operation	equipment	wip	flow time	time per
	MATCH	MATCH	1.6828	24.232	24.232
	ASSEMBLY	MATCH	5.4328	78.232	78.232

from operation	to operation	for each piece of good prodn: no. of pieces that are routed through this branch
DOCK	MATCH	1.0000
MATCH	ASSEMBLY	1.0000
ASSEMBLY	STOK	1.0000

details for individual equipment

Equipment name				
ICT	part name	oper	wip	utilization

				setup	run
	PCB149	LEVA	8.5355	8.333	41.67
	PCB259	LEVA	22.483	23.81	158.7
	PCB369	LEVA	13.610	16.67	83.33
Equipment name					
FNT	part name	oper	wip	utilization	
				setup	run
	PCB149	LEVB	7.5701	12.50	41.67
	PCB369	LEVB	7.5701	12.50	41.67
Equipment name					
PREB	part name	oper	wip	utilization	
				setup	run
	PCB149	PREB	12.255	12.50	41.67
	PCB369	PREB	16.630	12.50	83.33
Equipment name					
BI	part name	oper	wip	utilization	
				setup	run
	PCB149	BURN	277.78	2500.	.0000
	PCB369	BURN	277.78	2500.	.0000
Equipment name					
LEV2	part name	oper	wip	utilization	
				setup	run
	PCB149	LEV2	6.3273	13.89	46.30
	PCB369	LEV2	11.111	13.89	92.59
Equipment name					
INSP	part name	oper	wip	utilization	
				setup	run
	PCB149	INSP	14.609	4.630	92.59
	PCB259	INSP	16.931	7.937	119.0
	PCB369	INSP	14.609	4.630	92.59
Equipment name					
REPR	part name	oper	wip	utilization	
				setup	run
	PCB149	REPR	6.9444	.0000	.0000
	PCB259	REPR	7.1429	.0000	.0000
	PCB369	REPR	6.9444	.0000	.0000
Equipment name					
MATCH	part name	oper	wip	utilization	
				setup	run
	PCB	MATCH	1.6828	16.67	.0000
	PCB	ASSEMBLY	5.4328	12.50	41.67

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