

AN APPLICATION OF THE MULTI-PURPOSE SYSTEM SIMULATION (MPSS) MODEL TO THE MONITOR AND CONTROL DISPLAY SYSTEM (MACDS) AT THE NATIONAL AERONAUTICS AND SPACE ADMINISTRATION (NASA) GODDARD SPACE FLIGHT CENTER (GSFC)*

Fred W. Mill, George N. Krebs,
and Erwin S. Strauss,

Systems Sciences Division
Computer Sciences Corporation
Silver Spring, Maryland

ABSTRACT

The Multi-Purpose System Simulator (MPSS) model was used to investigate the current and projected performance of the Monitor and Control Display System (MACDS) at the National Aeronautics and Space Administration, Goddard Space Flight Center (NASA/GSFC), Greenbelt, Maryland in processing and displaying launch data adequately. MACDS consists of two interconnected mini-computers with associated terminal input and display output equipment and a disk-stored data base. MACDS serves as a two-way communications link between application host computers and terminal operators. The host computers handle network scheduling, launch monitoring, and vehicle maneuvers in real time.

Three configurations of MACDS were evaluated via MPSS and their performances ascertained. First, the current version of MACDS was found inadequate to handle projected launch data loads because of unacceptable data backlogging. Second, the current MACDS hardware with enhanced software was capable of handling two times the anticipated data loads. Third, an up-graded hardware ensemble combined with the enhanced software was capable of handling four times the anticipated data loads.

INTRODUCTION

This paper summarizes a study of projected performance of the current and future MACDS Digital Television (DTV) configurations in handling launch data loads at NASA's Goddard Space Flight Center, in Greenbelt, Maryland.

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The study was pursued to predict the increased load capacity of the proposed DTV Backup System (DTVBS) and to estimate quantitatively the amount of improvement in this system's performance over that of the current system. Additionally, the analysis indicated system components, both hardware and software, that may inhibit timely processing of incoming data blocks.

Three specific MACDS configurations were studied:

1. Current hardware with current software (called "current configuration").
2. Current hardware with enhanced software (called "transition configuration"). The major enhancements related to more efficient utilization of the data base disk unit via proposed changes in data blocking size and in distributive directory blocking.
3. Enhanced hardware with enhanced software (called the "DTV backup configuration" or DTVBS). The software enhancements were essentially those of the transition configuration. The hardware enhancements are detailed in the subsection entitled CONFIGURATIONS.

Each of these configurations was evaluated using the Multi-Purpose System Simulator (MPSS) model. For each configuration, MPSS was first executed for a nominal launch data load. The load was then successively increased until the system failed to process the arriving data in a steady-state condition. Supplementary runs were made to test sensitivity to the probabilistic fluctuations in the model, which were caused by the random-number generator. Sufficient excursions of the starting point of the random-number generator were executed to ensure convergence of values in the performance measurements. In this manner, the expected performances of the three configurations were directly compared.

System performance was declared to be intolerable if incoming data were backlogged at an average positive rate. Information was obtained on the apparent maximum data load at which each configuration backlogged. The particular elements in each configuration which caused data to backlog were identified during a detailed analysis of the model results. Performance parameters such as Central Processing Unit (CPU) idle time, data block response time, peripheral device data backlog and wait time, etc., pinpointed which components of the system were indicated as the factors limiting performance.

CONFIGURATIONS

HARDWARE CONFIGURATION

The hardware ensembles of the current and transition systems are identical, as depicted in Figure 1. Each contains a PDP-11/40 switch computer with unibus linkage to an extended memory unit and devices that interface with both the host computers and display computer. The display computer complex includes a PDP-11/40 computer with unibus linkage to an extended memory unit; two vector and character generators (VCGs) connecting the ensemble to the DTV screens; input keyboards; a Greenwich mean time (GMT) source; and a mass data storage disk drive. The backup system differs from the above by utilizing a PDP-11/70 display computer with a memory buffered through a high-speed cache accessible directly from the CPU or via the unibus (see schematic of the backup system as shown in Figure 2), a third VCG, and a faster mass data storage device.

Host computers were not simulated except as sources of input data to the modeled system.

DATA LOADS

The nominal traffic flux was set at a reasonably pessimistic (although not worst-case) level. This flux described a study scenario that corresponded to conditions during the busiest two-minute period of real-time launch support activity.

Data traffic was generated by four external sources: Goddard Real-Time System (GRTS) data via IBM System/360, Model 75s (360/75s); Goddard Trajectory Determination System (GTDS) data via a 360/95; Network Operations Control Center (NOCC) data via a Univac 642B; and Manual Insertions (MIs) via the DTV keyboards. Other data rates were negligible.

The GRTS primary traffic comprised Optical Projection Display Subsystem (OPDS) updates and DTV screen display pages. GTDS traffic consisted of occasional transmissions of display pages and data to be added to the data base. For both GRTS and GTDS, each display page was transmitted in a sequence of fixed-size blocks, with each containing header information. The number of blocks required per page was eight for the current configuration and two for the transition and backup configurations (incorporating enhanced blocking in the software). The primary NOCC data traffic comprised forced messages, display pages, and updates to pages. Each forced message resulted in a line of characters on the upper part of the display screen. The forced messages

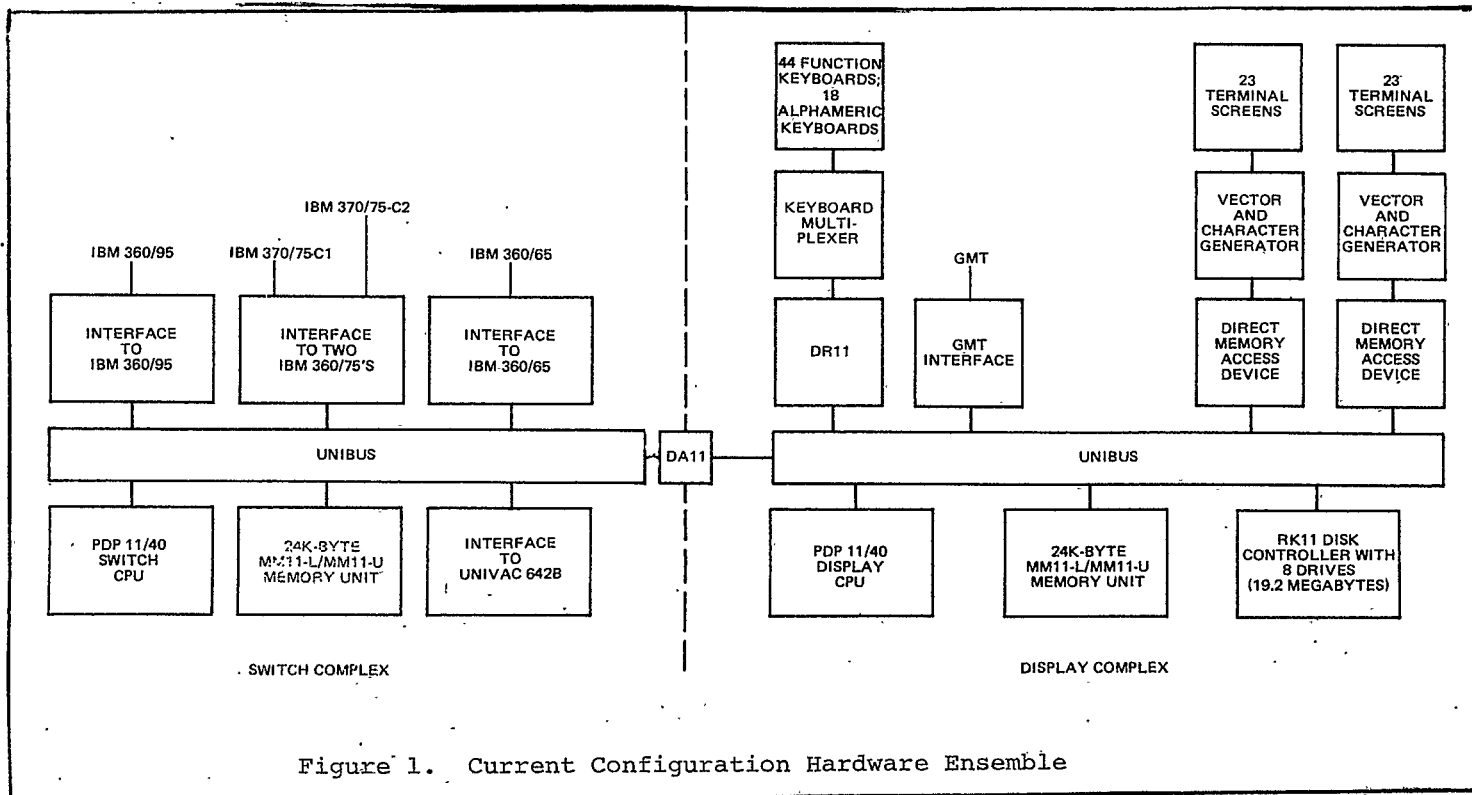


Figure 1. Current Configuration Hardware Ensemble

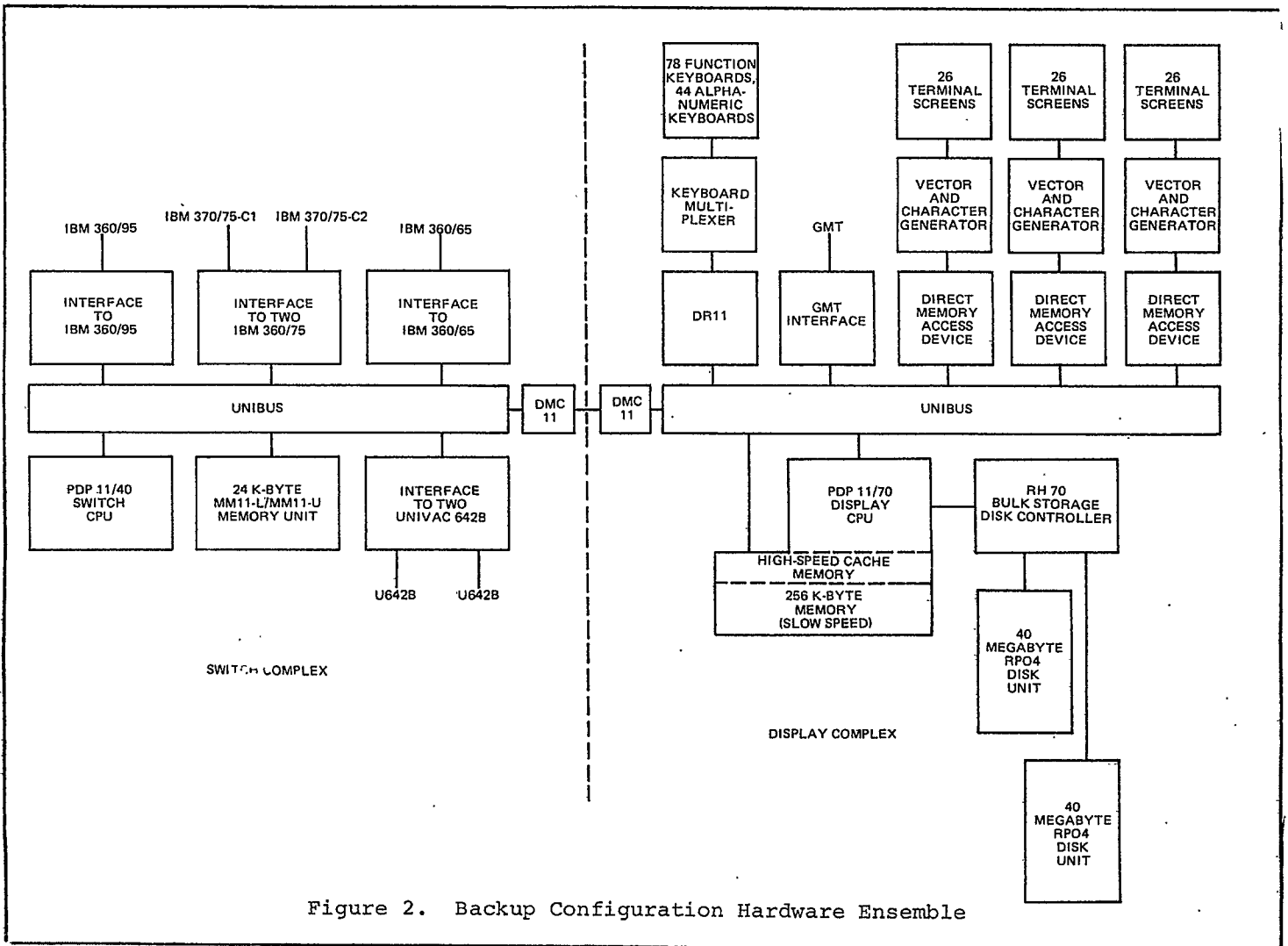


Figure 2. Backup Configuration Hardware Ensemble

appeared on all of the active display screens. Secondary data traffic from both GRTS and NOCC each comprised one acknowledgement and one retrieve data command per terminal input (MI) and three delete commands per minute.

Data traffic generated at the DTV terminals and the GMT source was estimated for the busiest two-minute interval as follows: 15 MIs per minute of 20 characters average size, 7 to GRTS and 8 to NOCC; 1 GMT update per minute; 3 retrieve commands per minute; and 1 terminal directory command (TDC) per minute. The logical flow of data blocks is illustrated in Figure 3. Each type of block was assigned a sequence of software modules which were serially executed. Each type of module specified the amount of CPU processing to be performed, module priority, and input/output (I/O) accesses.

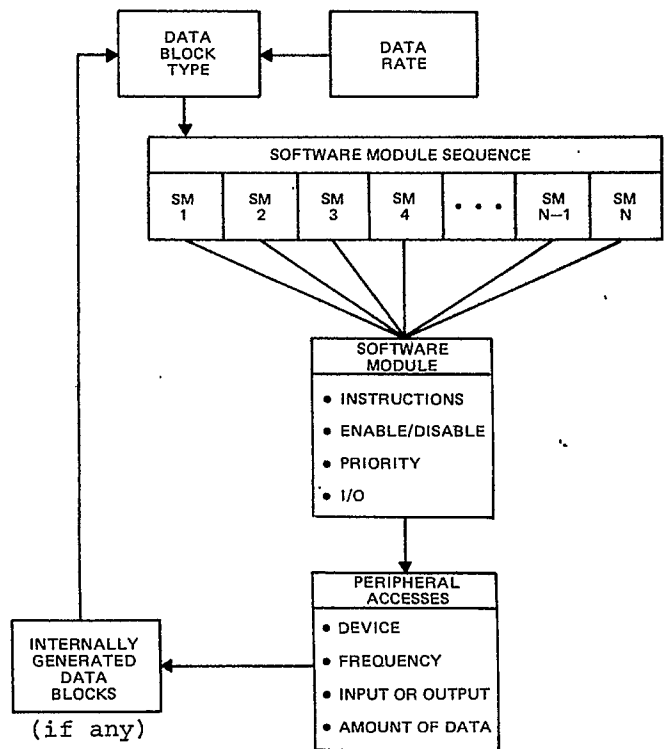


Figure 3. Data Block Flow Logic

Figure 5 shows the total data block backlog as a function of model simulation time for the three system configurations at various data rates. When the total backlog exceeded 100 (the current backlog capacity of the model), the simulation terminated. The assumption that a backlog greater than 100 implies a runaway situation is justified by the results. The one simulation where a large temporary backlog did occur -- the backup configuration at five times the nominal data rate -- differed from the simulations in which the 100 limit was exceeded. In the former case no significant backlog occurred during the first 60 seconds, and the backlog remained steady between 80 and 140 seconds. This indicated a system bordering between a runaway backlog and steady state processing. The latter cases started backlogging immediately and did not indicate any capacity to maintain real-time processing with increased simulation time.

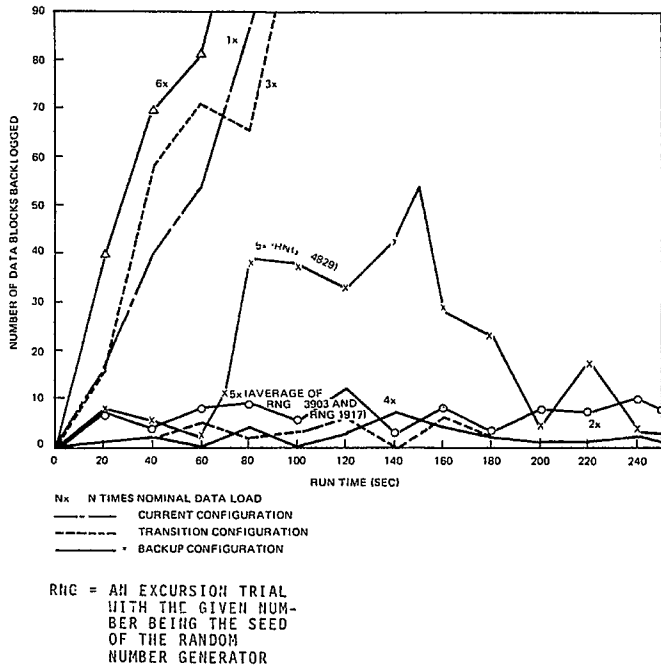


Figure 5. Data Backlogging

PERIPHERAL DEVICE AND CPU UTILIZATION

Statistical model results were obtained for the percentage of time the data base disk and the VCGs were busy when accessed during the simulation, and the percentage of time the CPU was utilized in executing software instructions.

The disk and VCG busyness statistic is computed as the number of times the particular device was busy when accessed, and multiplied by 100. The effect of device busyness is

reflected in the data backlog at the unit and the elapsed wait time for a block to be input or output. It should be noted that the busyness statistic is not equivalent to device utilization. This measure, which was not evaluated, would be the total time a device was utilized divided by the total run time.

The measure of interest concerning peripheral device and CPU utilization is the maximum data rate a configuration can handle. Maximum rates for the primary system components are given in Table 1 as multiples of the nominal rate. These maximum rates were estimated by extrapolating the percent busy statistics to the 100% busy value. In each configuration the data base disk is shown to be the constraining component.

Table 1. Maximum Data Rates Before Saturation

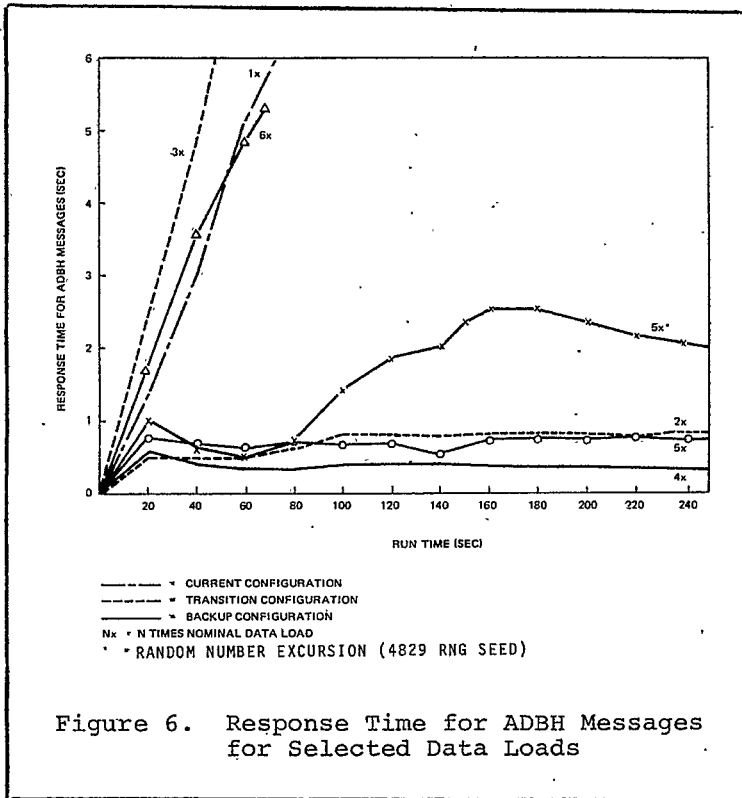
CONFIGURATION	CPU	DATA BASE DISK	VCGs
CURRENT	5	<1	~3
TRANSITION	~10	2	~5
BACKUP	~20	4	~9

DATA BASE RESPONSE TIME

The response time variation of data blocks as a function of data load is another parameter of interest in determining system performance. Of all the different data blocks in the modeled launch scenarios, the add-to-data-base (ADBH) data block is the best indicator of system performance degradation with increased data load. This data block type is the only one of substantial rate that requires I/O solely to the data base disk and not the VCGs as well. Since the data base disk is the device that backlogs first, the response time of this data block type rises in accordance with both data load and model run time for a load at or near system saturation.

Figure 6 shows the cumulative average response times at various data rates for ABDH messages for the three configurations as a function of simulated time during the computer run. The graph clearly shows that the average response time increases rapidly in cases where the configuration is saturating, and remains steady for data loads below the system's capacity. The statistical fluctuation and resultant data block backlog which occurred in the five times nominal data simulation of the backup system (with the 4829 random-number seed) results in an increase in response time as seen in the graph. An analogous effect in data block backlog for this scenario was already evidenced in Figure 5.

The response times of other data blocks which perform I/O to the data base disk also increase substantially when backlogging occurs. They were investigated in detail and showed an analogous behavior to the ADBH blocks.



CONCLUSION

The analysis indicates that the current configuration may not be able to maintain processing of a spacecraft launch in real-time. However, as indicated by the performance of the transition configuration, significant improvement appears possible by modifying DTEX software to preblock data going to the data base disk. The study indicated that the backup configuration appears to have an ample capacity to handle four launches simultaneously in real-time. All configurations evidenced adequate CPU capacity. The limiting component in each configuration appears to be the data base disk. The degree of performance inhibition by this device suggests that the capacity of each configuration might be doubled by the addition of a second data base disk controller.

The blocking changes embodied in the transition configuration software were first proposed after preliminary MPSS results for the current system indicated that the data base disk was the principal bottleneck. These changes eliminated the costly prospect of having to upgrade the current hardware merely to handle currently-expected data loads. The modeling study pinpointed areas of system enhancement needed to obtain improved performance. The MPSS model thus demonstrated its value as an effective tool for detailed analysis of computer systems.