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DIGITAL TWIN FOR DESIGN AND ANALYSIS OF CLUSTER TOOL IN WAFER FABRICATION

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ABSTRACT

In the semiconductor industry, many retrofits are being made to improve the production efficiency of manufacturing facilities. However, due to the nature of the data provided by the cluster tool, which is a semiconductor manufacturing facility, engineers have some limitations in utilizing it. To address this issue, it is necessary to introduce a digital twin model that can verify the performance of the semiconductor process cluster tool in a virtual environment, and to apply optimal mass production conditions based on this predictive data in the operational stage. In this study, we propose a digital twin model that visualize congestion factors during wafer transfer and evaluate the productivity of cluster tools.

1 INTRODUCTION

Manufacturing and supply chain management decisions in semiconductors are becoming increasingly critical, with each manufacturer striving to produce more products in the same period. Cluster tools, in particular, are advanced automation equipment used in these semiconductor manufacturing processes and are essential in the modern semiconductor industry due to the need for highly sophisticated and accurate wafer processing. However, due to the complex structure of a single cluster tool and the diversity of different models, it is difficult to manage and control the production floor. For some specific processes, wafer congestion needs to be strictly controlled, otherwise the quality of the wafers will suffer due to various factors such as residual gas and heat. To address these challenges, engineers have been making great efforts to identify and minimize the factors that contribute to wafer congestion in cluster tools through various retrofitting activities. This paper proposes the construction and application of a digital twin-based application that can run discrete event simulation of wafer transfer in a virtual environment based on actual facility parameters and process recipe data, and evaluate facility productivity through visualization and quantification of congestion factors in the cluster tool.

2 FRAMEWORK OF DIGITAL TWIN APPLICATION FOR CLUSTER TOOL

In the semiconductor manufacturing process, engineers monitor large amounts of sensor data and parameters from each cluster tool to control quality and maintain the efficiency of wafer production. However, the data provided by the cluster tools is often stored at regular intervals or only when certain events occur, which does not reflect the actual physical state and position of the wafers in detail. To address these issues, a framework for a digital twin-based application that can identify and analyze congestion factors in the wafer transfer process in detail is presented in Figure 1.

From the equipment engineering system (EES), the parameters of the physical cluster tool and the process recipe to be applied are sent to the digital twin application. The digital twin application synchronizes and

reflects them in the simulation model, and the virtual environment performs a discrete-event simulation of the manufacturing activity based on these data. Key statistics calculated based on the results of the simulation are stored back in the EES so that engineers can use them to predict future operations. In addition, when changes occur, such as facility retrofits and new processes, the model can be utilized to verify the production efficiency of optimal facility parameters and process recipes for each situation.

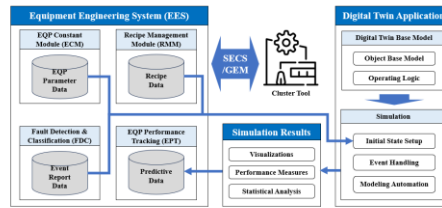

Figure 1: Framework of Digital Twin Application.

3 APPLICATION OF DIGITAL TWIN AND ONGOING WORK

The proposed digital twin application is implemented based on the specifications of a cluster tool that manufactures semiconductors in South Korea. The implemented digital twin simulates the same sequence as the actual process, based on the data operated in the actual process. Figure 2 shows an application that monitors the simulation of the digital twin in real time and visualizes key statistics in a dashboard that quantifies the time of congestion factors in wafer transfer based on the simulation results.

The digital twin application environment was developed in C# using Autodesk Inventor, Unity Editor 2021.3.21f1, and Visual Studio 2022. The data required to run the simulation is imported in the form of an Excel file and set as the parameters of the twin model, and the congestion time of each driving part of the wafer transfer process is measured in units of 0.01 seconds. Calculate the simulation results and visualize the key performance indicators such as cycle time of wafers, equipment occupancy, and wafer per hour expected to be processed in the process recipe in various formats. This allows engineers to evaluate the productivity of the cluster tool and utilize it for actual retrofitting activities.

In the current study, we conducted simulations based on the data of existing cluster tools and presented predicted results, but we are further researching and implementing AI-based reinforcement learning to propose optimal cluster tool parameters for productivity improvement.

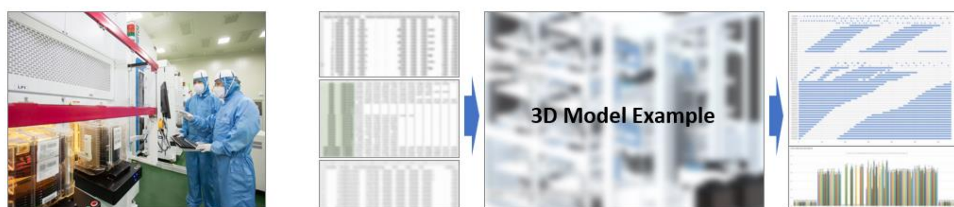

Figure 2: Cluster Tool with Engineers (left) and Digital Twin Application with Results Chart (right).

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