

## OPTIMIZED MANAGEMENT OF EXCURSIONS IN SEMICONDUCTOR MANUFACTURING

Justin Nduhura Munga  
Philippe Vialletelle

STMicroelectronics  
850 rue Jean Monnet  
38926 Crolles, FRANCE

Stéphane Dauzère-Pérès  
Claude Yugma

Ecole des Mines de Saint Etienne  
CMP – Site Georges Charpak  
880 avenue de Mimet  
13541 Gardanne, FRANCE

### ABSTRACT

In order to minimize yield losses due to excursions, when a process or a tool shifts out of specifications, an algorithm is proposed to reduce the scope of analysis and provide in real time the number of lots potentially impacted. The algorithm is based on a Permanent Index per Context (IPC). The IPC allows a very large amount of data to be managed and helps to compute global risk indicators on production. The information provided by the IPC allows for the quick quantification of the potential loss in the production, and the identification of the set of production tools most likely to be the source of the excursion and the set of lots potentially impacted. A prototype has been developed for the defectivity workshop. Results show that the time of analysis can be strongly reduced and the average cycle time improved.

### 1 INTRODUCTION

Semiconductor manufacturing is made of numerous and repetitive processing steps resulting in a significant cycle time of several weeks (Leachman and Ding 2011). With the increasing complexity and reduction in the size of devices, additional control steps are introduced in order to deliver products at high yield. This leads to increased cycle times and therefore time to market with the consequence of increased product prices. To stay competitive, companies have to provide pricing power against competitors to increase their market share. This implies a reduction in the number of controls without real added-value while achieving faster detection and elimination of yield limiting process problems.

The risk of adding or removing an inspection per time unit at a specific point in the flow depends on the information gained per inspection (Hall et al. 2008). This information can be the reduction of risk in terms of material at risk (uninspected lots since the last-known-good inspection) or the yield loss due to an excursion (when a process or a tool shifts out of specification). Once an excursion happens, it will continue to affect all wafers processing through the step performed by the affected tools until the problem is detected and containment actions taken. This implies additional controls and a very large amount of data to be managed in order to isolate as quickly as possible the source of the problem and the potentially impacted lots. Different techniques and solutions exist (Sajoto et al. 1999; Shindo et al. 1997; Minixhofer and Rathei 2005) but, with the increasing in complexity and the volume of data in high-mix semiconductor manufacturing, these techniques are seen impractical because of time and space consumption. As a consequence, a very large amount of lots are exposed until the problem is fixed.

In this paper, we propose a novel approach that aims at minimizing the yield losses due to excursions management. It consists in reducing the scope of analysis by providing as quickly as possible the set of production tools most likely to be the source of an excursion and the set of lots potentially impacted regarding the lot on which the excursion occurred. This information is computed with historical data based on the *IPC (Permanent Index per Context)* mechanism introduced in (Nduhura et al. 2011). A prototype has been developed and deployed in the defectivity area. The prototype displays the set of tools to be con-

sidered in the analysis and the set of lots potentially impacted regarding the lot on which the excursion occurred. Results show that the time of analysis can be strongly reduced and the cycle time improved.

The paper is structured as follows. Section 2 summarizes a literature review on excursion management in semiconductor manufacturing. In section 3, the problem is formulated. Section 4 describes the way excursion management can be optimized and Section 5 concludes the paper with recommendations for further research.

## **2 LITERATURE REVIEW**

(Wagner 2001) introduces the ten primary challenges identified by the International Sematech Product Analysis Forum for the future of the failure analysis in the semiconductor industry. Among these challenges, there are the cost of failures analysis and the complexity and volume of data. Failure site isolation is impacted by the cost of failure analysis since many of the most expensive tools are for failure site isolation (Gudmundsson and Shantikumar 2005). And the data required to support failure analysis is quite diverse, ranging from immediate needs such as test datalogs and layout databases to less frequently accessed data such as lot related information.

(Hall et al. 2008) provide a quality-cost model for excursion detection and reduction. Their results indicate that inspections can be allocated based upon the risk of yield excursions at defect limited process layers. With the aim of minimizing inspection while maintaining acceptable yield, (Sajoto et al. 1999) propose a methodology to optimize the use of inspection tools by utilizing in-line to end-of-line correlation to quantitatively measure the effectiveness of in-line inspections. (Lantz 2003) describes the methodology developed and used in the Cu CMP area of Intel's Fab 20 during the 0.13 mm logic technology production ramp. He indicates that a systematic application of manufacturing engineering principles leads to significant improvements of yield learning and excursion reduction. However, none of these articles give further explanation on the resource allocation and data management.

An algorithm or methodology can be efficient but impractical because of the amount and kinds of data to handle. (Yoshitake et al. 1998; Patel et al. 1996; Minixhofer and Rathei 2005; and Lee et al. 2006) work on inspection data management. The first article proposes an Automatic Killer Defect Selection (AKIDS) method for manipulating inspection data to reveal killer defects by analyzing defect sizes and killer defect judgment rules based on pattern dimensions. The second article proposes a computer integrated manufacturing system for excursion management. The way various elements of an excursion management system can be integrated and automated for material containment and risk assessment is described. The third article suggests the use of Technology Computer-Aided Design (TCAD) for fast analysis of misprocessed wafers and yield excursions. The last article proposes K-means clustering for classifying wafers into various types of failures. In these four papers, authors clarify the importance of data management in excursions analysis. However, they do not explain the technical aspects when implementing different solutions. Complexity, time of analysis, and resource management can have a strong impact on the overall cycle time.

Close to our work are the studies of (Shindo et al. 1997; Shindo et al. 1999; Pepper et al. 2005). The first two papers propose a methodology for identifying the source of excursion using defect type Pareto. By grouping a class of defect with the killer class, their result show that it is possible to guess the potential source of the excursion and prioritize the problem fixing procedure. (Pepper et al. 2005) propose a classification scheme based on the optical attributes of inline, low resolution images in order to separate killer defects from non-killer ones. This allows lots to be automatically flagged and accelerated for further analysis. Concerning the large amount of data management, (Dauzère-Pérès et al. 2010) and (Nduhura et al. 2011) introduce novel approaches for real-time risk management. We now extend these previous research works and apply them to an optimized management of excursions.

### 3 PROBLEM FORMULATION

A defect source which is not immediately isolated has a very strong impact on both yield and cycle time. Let us take a simplified example to illustrate the purpose. The processing flow described in Figure 1 illustrates the case where a lot L1 has to be processed successively in the CMP (Chemical Metal Polishing), PHOTO, and ETCH workshops before being measured in the defectivity workshop.

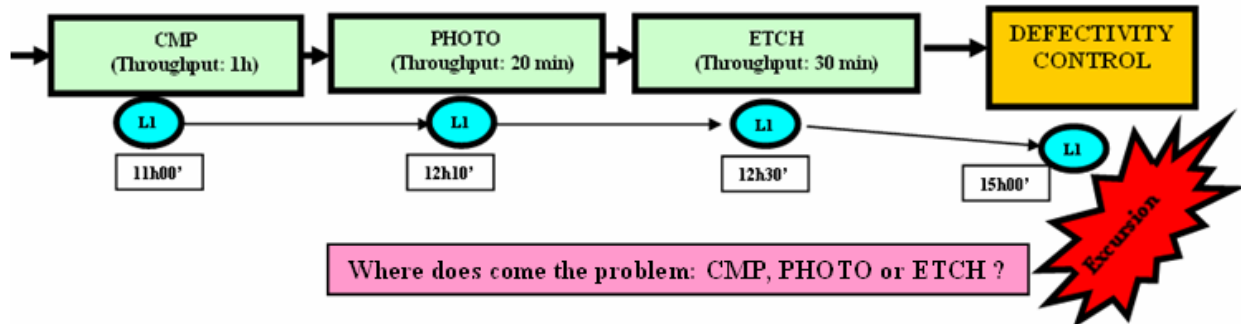


Figure 1: Example of an excursion management problem

As illustrated in Figure 1, when lot L1 arrives in the defectivity workshop, a control is performed on lot L1 in order to obtain information on production tools (CMP, PHOTO, and ETCH production tools). If the defectivity control performed on lot L1 is out of specifications, an excursion occurs. The challenge is therefore to find the excursion source as quickly as possible without stopping the production. This implies to:

- Isolate the most probable source of excursion (CMP, PHOTO, or ETCH?),
- Select the best set of lots to measure in order to contain the excursion,
- Quantify the number of lots impacted.

Depending on the time between the excursion detection and the source isolation, the impact can be significant. In Figure 1, the throughput on the CMP production tool is 1 hour and 20 minutes for the PHOTO production tool and 30 minutes for the ETCH tool. Lot L1 has been processed on the CMP tool at 11h00 and measured in the defectivity workshop at 15h00. It means that 4 hours elapsed between the process of lot L1 on the CMP tool and its measurement in defectivity. This corresponds to the process of 4 lots on the CMP tool (one hour for each lot). In other words, when an excursion occurs on lot L1 in the defectivity workshop, there are at least 4 lots potentially impacted regarding the CMP tool.

If the defect source is isolated 10 hours later, we have 14 hours (4 + 10) between the process of lot L1 on the CMP tool and the source isolation. This implies that there are 14 lots potentially impacted instead of 4 lots. In the case where the process operation is non-reversible, it will result in 14 lots, each containing 25 wafers, which results in 350 wafers impacted regarding the CMP workshop. The same for all production tools on which lot L1 has been processed before arriving in the defectivity workshop.

One of the complexities in isolating the defect source in high-mix semiconductor manufacturing comes from the large amount of data to handle as quickly as possible. Most of the time, engineers are used to navigate between different IT tools and use their experience to identify the most probable cause of the excursion. Once the most probable cause of defect is identified, the next step consists in determining and selecting a lot or a set of lots to measure in order to confirm or deny the excursion. Depending on the current processing step on a lot, the recipe, the technology, the WIP (Work In Progress), the lot history, the product, etc., a commonality analysis is performed in order to choose a lot or a set of lots to measure. As a result, a lot is chosen based mainly on its similarity with the lot on which an excursion has occurred. This implies an increasing of risk on the set of lots potentially impacted.

To tackle this problem, key parameters must be determined as quickly as possible in order to reduce the scope of analysis and take rapid actions on lots potentially impacted. For that, we use the IPC information introduced in (Nduhura et al. 2011) to collect and compute in real-time a very large amount of data based on various risk indicators.

#### 4 OPTIMIZING EXCURSION MANAGEMENT

The approach developed in this section is based on real-time risk indicators computed with the *IPC* mechanism. Let us recall our work.

##### 4.1 IPC Mechanism

The Permanent Index per Context (*IPC*) is a counter which is increased each time a context is verified. The context can be a tool, a chamber, a recipe, a technology, a resin, the combination of an operation and a technology, etc. This counter is never reset except when a special event occurs (Preventive Maintenance, intermediary qualification, etc.).

The context here is defined at the equipment level in order to control the risk on production tools. The risk is evaluated as the number of wafers processed on a production tool since the last control performed. To each lot  $l$  and tool  $m$  is associated a Permanent Index per Context (*IPC*), which is equal to 0 if  $l$  is not processed on  $m$ . Let  $M$  be the number of production tools, and  $NW(l)$  be the number of wafers in lot  $l$ . The goal is to update in real time the following parameters:

- $LLM(m)$  : Index of the Last Lot that has been Measured for production tool  $m$ ,
- $IPC_l^m$  : *IPC* of lot  $l$  for production tool  $m$ .

Using these parameters, it is possible to calculate the following indicators:

- $NI_l^m$  : The Number of wafers potentially Impacted on tool  $m$  if lot  $l$  was measured,
- $NI_l$  : The Number of wafers Impacted on all production tools if lot  $l$  was measured.

When lot  $l$  is processed on production tool  $m$ , an  $IPC_l^m$  is associated to  $l$ , which is equal to the *IPC* of the lot  $l'$  processed just before  $l$  on tool  $m$  plus the number of wafers in  $l$ :

$$IPC_l^m = IPC_{l'}^m + NW(l) \quad (1)$$

The risk indicator on a production tool  $m$  is then given by:

$$RI_m = IPC_l^m - IPC_{LLM(m)}^m \quad (2)$$

Using the *IPC* information, it is possible to quantify the number of lots potentially impacted whenever a problem occurs on a lot  $l$ . This number can be determined for a given production tool  $m$  ( $NI_l^m$ ) and for all production tools ( $NI_l$ ):

$$NI_l^m = \max(0, IPC_l^m - IPC_{LLM}^m) \quad (3)$$

and

$$NI_l = \sum_m NI_l^m \quad (4)$$

### 4.2 Excursion management

When an excursion occurs after a defectivity control, the analysis is divided into two main steps:

- Identification of the tool most likely to be the source of the problem,
- Selection of the best set of lots to measure in order to fix as quickly as possible the origin of the problem. This information will help to quantify the number of lots impacted and take decisive actions regarding the current status in the fab.

Based on the example described in Figure 1, let us introduce another example in Figure 2 to understand the scope of analysis when an excursion occurs.

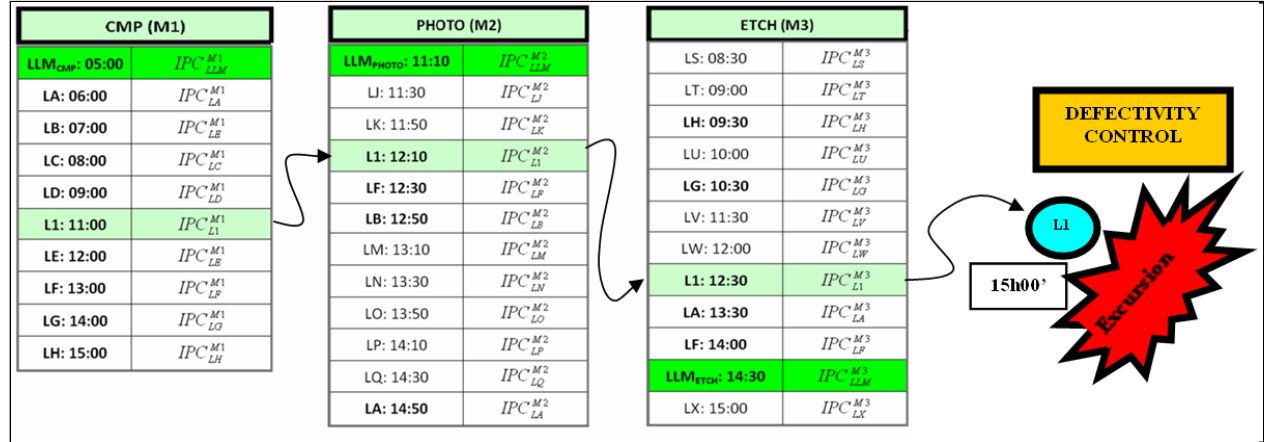


Figure 2 - Example of excursion analysis

In the example described above, lot L1 is processed on three different process tools before being detected as bad in defectivity. Depending on the state of each production tool, the scope of analysis can be reduced based on the last control performed. Reducing the scope of analysis implies a reduction in the number of data to manage and therefore a reduction in the time of analysis. Figure 2 shows the history of each process tool on which lot L1 has been processed. What we can see is that, for process tool ETCH(M3), a control (LLM<sub>ETCH</sub>) was performed after the process of lot L1. The scope of analysis can therefore be reduced to the process tools CMP(M1) and PHOTO(M2) if the last control performed on ETCH(M3) was within specifications. This information can easily be obtained and in real-time with the IPC indicator.

Let us introduce some notations:

- $LE$  Index of the Lot on which the Excursion has occurred,
- $M_{LE}$  The set of Machines on which lot  $LE$  has been processed,
- $MI_{LE}$  The set of Machines to be considered in the analysis,
- $LPI_{LE}^m$  The set of Lots Potentially Impacted regarding lot  $LE$  on production tool  $m$ ,
- $LPI_{LE}$  The set of Lots Potentially Impacted regarding lot  $LE$  in the entire production.

According to (1), (2) and (3), we have:

$$MI_{LE} = \{m \in M_{LE} \mid NI_{LE}^m > 0\} \quad (5)$$

$$LPI_{LE}^m = \{i \in \{1, \dots, L\} \mid IPC_i^m < IPC_{LE}^m \text{ and } NI_i^m > 0\} \quad (6)$$

$$LPI_{LE} = \bigcup_{m=1}^{M_{LE}} LPI_{LE}^m \quad (7)$$

For the case illustrated in Figure 2, the set of lots potentially impacted is given by:

$$\begin{aligned} LPI_{L1} &= \{PI_{L1}^{M1}\} \cup \{PI_{L1}^{M2}\} \cup \{PI_{L1}^{M3}\} \\ &= \{A, LB, LC, LD, LE, LF, LG, LH\} \cup \{J, LK, LF, LB, LM, LN, LO, LP, LQ, LA\} \\ &= \{A, LB, LC, LD, LE, LF, LG, LH, LJ, LK, LM, LN, LO, LP, LQ\} \end{aligned}$$

Once the set of lots potentially impacted is determined, the challenge is to find the best lot to measure in order to fix the source of excursion while providing the as much information as possible on the set of lots potentially impacted. A first prototype has been developed. The prototype displays the set of machines to be considered in the analysis and the set of lots potentially impacted as described above. Using this prototype, we observed that the time of analysis could be strongly improved.

## 5 CONCLUSIONS AND PERSPECTIVES

In this paper, an optimized management of excursions is proposed. It is based on a Permanent Index per Context (*IPC*) and aims at providing in real time the set of production tools most likely to be the source of the excursion and, depending on the lot on which the excursion occurred, providing the set of lots potentially impacted. The *IPC* allows a very large amount of data to be managed with very little resource usage.

A prototype has been developed for the defectivity workshop at the 300mm plant of STMicroelectronics in Crolles in order to reduce the scope of analysis and therefore find as quickly as possible the origin of the excursion while minimizing the risk on lots potentially impacted. Results show that the overall cycle time can be decreased thanks to the reduction of data to manage, and that the impact on the lots at risk is lowered.

However in this first implementation, the global information brought by each lot regarding the set of lots potentially impacted is not provided. The amount of data to analyze can increase depending on the step of control and the current situation in production. It could therefore be interesting to propose one or several indicators to choose the best lot (or lots) to measure depending on the probability for each tool of being the source of the excursion.

Future work will be dedicated to the definition of such indicators and the integration of other parameters such as the time of measurement and the criticality of the different process operations.

## ACKNOWLEDGMENTS

This work has been done within the framework of STMicroelectronics. The scientific part of the work has been done within the framework of Centre Microélectronique de Provence, site George Charpak of the Ecole Nationale Supérieure des Mines de Saint Etienne in Gardanne, France.

## REFERENCES

Dauzère-Pérès, S., J.-L. Rouveyrol, C. Yugma, and P. Vialletelle. 2010. "A Smart Sampling Algorithm to Minimize Risk Dynamically." *IEEE Advanced Semiconductor Manufacturing Conference and Workshop*: 307–310.

- Gudmundsson, D., and G. Shantikumar. 2005. "Improving the deployment of inspection tools; tutorial on inspection capacity and sample planning." *IEEE International Symposium on Semiconductor Manufacturing*: 410–413.
- Hall, G. D. R., R. Young, M. Dunne, and M. Muro. 2008. "A quality-cost model of in-line inspections for excursion detection and reduction." *IEEE Advanced Semiconductor Manufacturing Conference and Workshop*: 273–277.
- Lantz, S. 2003. "An Effective Methodology for Improving Equipment Reliability and Reducing Excursions During a Factory Ramp." *IEEE Advanced Semiconductor Manufacturing Conference and Workshop*: 297–302.
- Leachman, R. C., and S. Ding. 2011. "Excursion Yield Loss and Cycle Time Reduction in Semiconductor Manufacturing." *IEEE Transactions on Automation science and engineering*. Vol. 8: 112–117.
- Lee, C. H., H. D. Woo, S. W. Hong, J. Y. Moon, S. H. Kang, J. C. Lee, K. W. Chong, and K. S. Oh. 2006. "Novel Methods for Identification and Analysis of Various Yield Problems in Semiconductor Manufacturing." *IEEE Advanced Semiconductor Manufacturing Conference and Workshop*: 185–190.
- Minixhofer, R., and D. Rathei. 2005. "Using TCAD for Fast Analysis of Misprocessed Wafers and Yield Excursions." *IEEE Advanced Semiconductor Manufacturing Conference and Workshop*: 197–199.
- Nduhura Munga, J., S. Dauzère-Pérès, P. Vialletelle, and C. Yugma. 2011. "Dynamic Management of Controls in Semiconductor Manufacturing." *IEEE Advanced Semiconductor Manufacturing Conference and Workshop*.
- Patel, D. N., D. Core, H. N. Nguyen, G. Martin, K. Mooney, G. Neri, and D. Cresswell. 1996. "A computer Integrated Manufacturing System for Excursion Management." *IEEE Advanced Semiconductor Manufacturing Conference and Workshop*: 23–25.
- Pepper, D., O. Moreau, and G. Hennion. 2005. "Inline Automated Defect Classification: a Novel Approach to Defect Management." *IEEE Advanced Semiconductor Manufacturing Conference and Workshop*: 43–48.
- Sajoto, D., A. Gordon, A. McCauley. 1999. "Inspection Optimization for Excursion and Baseline Defect Monitoring in a Manufacturing Environment." *IEEE International Symposium on Semiconductor Manufacturing*: 371–374.
- Shindo, W., E. H. Wang, R. Akella, and A. J. Strojwas. 1997. "Effective Excursion Detection and Source Isolation with Defect Inspection and Classification." *IEEE Transactions on Semiconductor Manufacturing*: 146–149.
- Shindo, W., E. H. Wang, R. Akella, A. J. Strojwas, W. Tomlinson, and R. Bartolomew. 1999. "Effective Excursion Detection by Defect Type Grouping Inspection and Classification." *IEEE Transactions on Semiconductor Manufacturing*. Vol. 12: 3–10.
- Wagner, L. C. 2001. "Failure Analysis Challenges." *IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits*: 36–41.
- Yoshitake, Y., S. Maeda, and K. Watanabe. 1998. "Defect Control Using an Automatic Killer Defect Selection Method." *IEEE International Workshop on Statistical Metrology*: 32–35.

## AUTHOR BIOGRAPHIES

**JUSTIN NDUHURA MUNGA** received his Engineering degree in Computer science, Microelectronics, and Automation from the Ecole Polytechnique de Lille in Lille, France in 2009. Currently he is a Ph.D. student in Industrial Engineering at the Ecole des Mines de Saint-Etienne in Gardanne, France, and works at STMicroelectronics in Crolles, France. His email address is [justin.nduhura-munga@st.com](mailto:justin.nduhura-munga@st.com).

**STEPHANE DAUZÈRE-PERÈS** is Professor at the Provence Microelectronics Center of the Ecole des Mines de Saint-Etienne, where he is heading the Manufacturing Sciences and Logistics Department. He received the Ph.D. degree from the Paul Sabatier University in Toulouse, France, in 1992; and his Habili-

tation à Diriger des Recherches from the Pierre and Marie Curie University, Paris, France, in 1998. He was a PostDoc Fellow at the Massachusetts Institute of Technology, U.S.A., in 1992 and 1993, and Research Scientist at Erasmus University Rotterdam, The Netherlands, in 1994. He has been Associate Professor and Professor from 1994 to 2004 at the Ecole des Mines de Nantes in France. He was invited Professor at the Norwegian School of Economics and Business Administration, Bergen, Norway, in 1999. Since March 2004, he is Professor at the Ecole des Mines de Saint-Etienne. His research mostly focuses on optimization in production and logistics, with applications in planning, scheduling, distribution and transportation. He has published more than 35 papers in international journals and 100 communications in conferences. His email address is [dauzere-peres@emse.fr](mailto:dauzere-peres@emse.fr).

**CLAUDE YUGMA** is an Associate Professor at the Ecole des Mines de Saint-Etienne, in the Manufacturing Sciences and Logistics Department. He received the Ph.D. degree from the Institut National Polytechnique de Grenoble, France, in 2003. His email address is [yugma@emse.fr](mailto:yugma@emse.fr).

**PHILIPPE VIALLETTELLE** is manager of the Operations and Methods System group at STMicroelectronics. After receiving an Engineering degree in Physics, he entered the semiconductor industry working on ESD and physical characterization. His next experiences were Metrology and Process Control where he drove the deployment of methodologies and tools for a 200mm fab. He finally integrated Industrial Engineering and is now responsible for the development of advanced programs for the management of Crolles 300mm production line. At European level, Philippe is in charge of the definition and follow-up of collaborative programs in the field of Manufacturing Sciences such as HYMNE or IMPROVE. His email address is [philippe.vialletelle@st.com](mailto:philippe.vialletelle@st.com).