ANALYSIS OF MULTIPLE PROCESS FLOWS IN AN ASIC FAB WITH A DETAILED PHOTOLITHOGRAPHY AREA MODEL

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ABSTRACT

ASIC fabs are characterized by multiple process flows. This is mainly due to the highly diversified product portfolios within such fabs. In this study, we first examined the cycle time for individual process flows in a medium volume ASIC fab. We compared these process flows in terms of overall cycle time and using a cycle time index. Secondly, focusing on photolithography we developed a simulation model that employs cycle time data to analyze the impacts of process flow diversity. Thirdly, we used this model to examine the impact on cycle time of changing the volumes of wafer starts on different process flows. The detailed results of simulation experiments along with the concluding remarks are given at the end of the study.

1 INTRODUCTION

High product mixes with low volume customized products such as System-on-Chip (SOC) are the main characteristics of Application Specific Integrated Circuit (ASIC) fabrication plants. Within such fabs, multiple process flows are present largely due to the variable product life cycles, rapidly changing technology, and the need for controlling the fab costs (Neacy et al. 1993). From an operational point, more diverse ranges of products bring more variability into the wafer fabrication and necessitate more versatile resources which complicate the fab operations even further.

This study uses a simple global fab model that contains a detailed photolithography module to analyze different aspects of multiple process flows. Particularly, this study evaluates single flows, multiple flows in equal volumes and also multiple flows in varied volumes. Cycle time performance and equipment utilizations with regard to photolithography are investigated within this framework.

The organization of this paper is as follows. In Section 2 we describe the fab operations that form the basis for the simulation study that follows. Section 3 presents the simulation conceptual model that was implemented. In

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section 4, results from input data analysis on pass times is described. Section 5 presents the simulation model, while section 6 presents the results from the experiments.

2 PHOTOLITHOGRAPHY AREA

Photolithography is one of the most constraining elements of the wafer fabrication process. This is mainly due to the high capital investment requiring high tool utilization. Dynamic re-entrant flows add further complexity. The photolithography process consists of three main steps, which are coat, expose and develop. In "coat", the wafer is coated with a photoresist material, which is a type of light-sensitive polymer. Then in the "expose" step, the wafer is exposed with ultraviolet light (UV) in order to print the circuit pattern onto the wafer. This is done using a reticle, which is a chrome patterned glass that defines the circuit pattern. This pattern tends to be unique for each layer. In "develop", the exposed sections are dissolved away in order to remove the photoresist material on the exposed sections of the wafer. In the literature many studies have examined the effects of the photolithography area on cycle time management by employing different operational control rules such as setup policies, machine assignment strategies and dispatching rules (see Spence and Welter (1987); Akcali, Nemoto, and Uzsoy (2001); Monch, Prause, and Schmalfass (2001)). With regard to the product mix, Neacy et al. (1993) compare multiple process scenarios with the single process flow fabs by estimating relative cost. Park et al. (1999) report that increased product mix homogenity causes higher cycle time due to the increased reticle utilizations. Dummler (2000) examines the effect of altering the weekly product mix on the short term fab performance. Iwata and Wood (2000) introduce a general cost model for the ASIC fabs and they consider fab capacity and process diversity explicitly. Apart from these studies, however, not many research studies considered the interaction of process flows especially in a high mix ASIC environment. In this study,

we address this problem with a detailed simulation model of the photolithography area.

3 CONCEPTUAL MODEL

This study started with a conceptual model designed to better structure the simulation model and corresponding data requirements gathering (Robinson 2006). The conceptual model for the system to be analyzed includes a simplified version of the wafer fabrication plant that includes five different modules in wafer fabrication. These modules are: start/release, first delay, photolithography loop, second delay, third delay and exit (Fab operation). Figure 1 shows the sketch of conceptual model.



Figure 1: Sketch of conceptual model.

In the start/release module, lots are released into the system based on a weekly release plan. The input information consists of the sequence of the photolithography steps for each process flow, weekly release plan of products and product mix (i.e., percentages of process flows). The first delay represents the time from release to the first entrance of the lots into the photolithography area. All the process steps from release to the first visit of photolithography area are combined together. The input information for this module consists of the time that a lot spends from release to the first entrance of photolithography area for each process flow. The photolithography module consists of a number of tool sets. The required information in this module includes the capability of tool sets for each process flow, recipes for different process flows and processing times for each process flow step. The second delay module models the delay from exiting photolithography to entering it. The number of passes through the photolithography area is variable depending on each process flow. The input information for the second delay module consists of the time that a lot spends from exit to next entrance of the photolithography area for each process flow. The last module, the third delay represents the time that a lot passes through from the last exit of photolithography tool to the shipping area in the wafer fabrication plant. As before, all the steps from the last photolithography exit to the shipping area are combined together.

This model provides a framework to analyze the effect of photolithography performance on the cycle time index across multiple process flows. The total cycle time of a lot is defined as the time a lot spends from exiting the first delay to the time a lot enters to the third delay. The cycle time index is obtained by dividing the total cycle time by the number of mask layer passes for each process flow. The photolithography area performance is observed using the tool utilizations and tool wait times in this area.

Similar conceptual models are given in the literature in the studies of Peikert et al. (1998), Nayani and Mollaghasemi (1998), Park et al. (1999), Rose (2000) and Rose (2007). Peikert et al. (1998) emphasize the feasibility of modeling a focused single area from a whole plant. They consider the delays as "dummy work stations" with an infinite number of servers to analyze photolithography operations. Each workstation has a process time from the triangular distribution and a delay time calculated using a cycle time factor. Nayani and Mollaghasemi (1998) modeled the dummy work stations with constant delays. While, Park et al. (1999) use exponential delay times with different mean values. Further, Rose (2000) considers a similar conceptual model that uses Gamma variates for delay distributions. He compares the simple fab model with a full fab model in a number of ways such as cycle time prediction, lot overtaking and correlation between cycles. Also, delay time distributions which vary according to current inventory levels are used instead of fixed delay distributions in the paper of Rose (2007).

4 INPUT DATA ANALYSIS

Detailed analysis was carried with the main aim of characterizing the performance of different process flows in the fab.

4.1 Data Collection

Real fab data were collected for a sample of process flows. Collected data included all steps of these process flows in the wafer fabrication. Each lot step under each process flow covers queue time, step end time, step start time, run time and wait time. Due to the nature of semiconductor manufacturing, a process flow can consist of more than 300 steps. For this reason, many products may have manufacturing lead times greater than two months.

4.2 Sampling of the Lots

In sampling, lots were selected with release dates that differed by at least one week. The reason is that system variability can be better reflected if lots are sampled from different release dates.

4.3 Data Analysis Steps

Data analysis starts with sorting the fab data for a particular process flow based on the queue times. Then a certain number of lots having a complete set of steps from start (release) to finish (shipping area) are found by filtering. All the photolithography visits of lots and all related times are found by filtering the data for the photolithography area for each lot. At the end, different delay (pass) times are calculated for each sample lot under each process flow. The same procedure is performed to obtain process times for each lot. To illustrate, a graph of process flow A is given in Figure 2. It is important to note that all the results are manipulated for proprietary reasons in the figures and tables.

Figure 2 shows pass times of sample lots for process flow A. The pass times in the figure are calculated by taking the difference between the the time of the last exit and the next visit to the photolithography area of a lot. As can be observed in Figure 2 peaks can be observed at certain passes. In particular, there are peaks at passes 2, 9, 10, 19 and 21. These peaks are primarily due to the longer intrinsic times of these stages.



Figure 2: Pass times in process flow A.

4.4 Assumptions on data analysis

In the data analysis, lots having the same release dates are not considered. Rework steps are not taken into account and they are deleted from the data. Also, a homogenity test for pass values is performed. Some outliers representing exceptionally high and low values are removed from the data after the comparison of the lots from the same process flow. In addition, a correlation analysis is performed for each process flow, and an implicit assumption is made on all pass times as they are considered to be independent of each other. Finally, the histograms of pass times are fitted into distributions to obtain delay distributions. Gamma distributions with shape (α), scale (β) and location (γ) parameters are used for the first and third delays. However, separate distributions are used for each process flow in the second delays. The descriptive statistics of process flows are given in Table 1.

Table 1: Descriptive statistics for each process flow.

Flow	Cf. Var	S	K
1st Delay	0.60	1.94	3.30
А	1.31	3.20	11.87
В	1.26	3.22	11.63
С	1.24	3.00	9.72
D	0.92	1.67	2.97
E	1.38	2.81	8.36
F	1.96	7.89	67.89
G	1.56	3.16	10.16
Н	0.97	1.49	2.50
3rd Delay	0.75	1.65	2.53

In Table 1, the first column shows the coefficient of variation (Cf. Var) values. According to the results, relatively lower variations are observed in the first and third delays than the second delays. The second delay is examined as a function of process flows and process flow F shows the highest variation. With regard to the second and third columns which represent the skewness (S) and kurtosis (K) values, the first delays, process flow D, H and third delays have moderate skewness and kurtosis. The process flows A, B, C, E and G have slightly higher skewness and high kurtosis values. This is also in accordance with higher coefficient of variance values. However, process flow F has the highest kurtosis, skewness and coefficient of variation values. The reason is that much of the variance comes from extreme values instead of frequent normal sized deviations in process flow F.

5 SIMULATION MODEL

A simulation model was built using eM-Plant 7.5 simulation software by Tecnomatix (2007). The model was developed using the conceptual model described in Section 3. This section explains the simulation model assumptions and the simulation experiments.

5.1 Simulation Model Assumptions

The simulation model assumptions include assumptions on part mix, release mechanism of products, capabilities and processing times of tools, and dispatching in the photolithography area.

Product mix consists of eight different product types. The base simulation model percentages are given in Table 2 below. In reality, these quantities and percentages for the flows in the fab change depending on customer demand. Also, the table is manipulated for proprietary reasons.

Process	Weekly Release	Part Mix	
Flows	Quantity (wafers)	Percentage (%)	Passes
А	175	17.5	29
В	175	17.5	25
С	175	17.5	36
D	125	12.5	23
E	125	12.5	18
F	125	12.5	29
G	50	5	31
Н	50	5	20
TOTAL	1000	100	

Table 2: Simulated product mix based on main process flows.

Daily release of products is based on two 12 hour shifts (2x12hrs). The wafers are released in lot sizes of 25 wafers at the beginning of each shift and the maximum release quantity is 100 wafers or 4 lots per shift. This makes a maximum of 200 wafers (8 lots) per day based on the given product mix percentages. The system is assumed to be in operation 7 days a week. There is no priority in releasing the products. The products are selected randomly based on their cumulative part mix percentages. In the real system, selection of parts depends on many factors including subsequent batch processing effects etc. However, this situation is disregarded in this model. At the end of each week, release quantities of each product should meet the weekly release quantities given in Table 2.

The tools in the photolithography area have 100 % availability, and they are assumed to be nonidentical tools. In other words, they have different capabilities based on product recipes. A capability check is performed automatically when a lot enters the photolithography queue. A capability table is illustrated as an example in Table 3 below. In the capability table, "1" shows that the tool has the capability for a particular recipe and capability is turned on this tool. "0" shows that the tool does not have the capability for that recipe and capability is turned off on the tool. The capabilities of tools in percentages are also given for each process flow in Table 4. To illustrate, Tool 1 has a capability of 69 % for process flow A. That is, if 29 recipes for all layers are required, only 20 of them have the capability on Tool 1. In addition, the tools have different deterministic processing times ranging from 35 to 50 wafers per hour (WPH). However, operators, reticles and machine failures are not included in the model.

The first, second and third delays (see Figure 1) are modeled using infinite parallel identical servers. Delay times were obtained from the input data analysis described in Section 4. The delay durations in the second delay are a function of the process flows while in the first and third

Table 3: Tool capabilities by recipes.

Recipe	Tool 1	Tool 2	Tool 3	Tool 4	Tool 5
xxA01	1	0	1	1	1
xxB03	1	0	0	0	1
xxC05	0	1	0	1	0
•	•	•	•	•	•

Table 4: Capabilities of tools under each process flow.

	Tool Capabilities (%)				
Flows	Tool 1	Tool 2	Tool 3	Tool 4	Tool 5
А	69	82	42	82	82
В	90	81	31	69	81
С	96	93	73	84	93
D	83	83	78	83	83
E	100	100	21	15	100
F	91	91	76	91	91
G	100	100	30	26	100
Н	100	100	19	13	100
TOTAL	80	83	44	58	83

delays they are not. The dispatching in the photolithography area is based on First-In First-Out (FIFO) rule. The same rule is applied for the delay areas in the model as well. In practice, the dispatching policy depends on first priority checks and then FIFO rule check.

5.2 Simulation Experiments

Pilot simulation runs with different simulation lengths show that three months is adequate to remove the initialization bias based on daily throughputs. Simulation length is determined as three years to capture the steady-state behaviour of the system. As for the model validation, a structured walk-through and comparison of the cycle time (CT) per layer of each process flow with the historical fab data were performed. The main performance measure of interest in the simulation experiments is the cycle time (CT) index for each process flow and the overall CT index which is considered as the weighted average cycle time per layer. The other performance measures are the photolithography tool utilizations and wait times.

Performance measures are obtained by running 10 replications with different seed values. Three different experimental sets (S1, S2 and S3) are performed in order to analyze the single process flows, the effects of increasing product diversity, and to analyze interaction of multiple process flows at different start volumes. The first experimental set (S1) includes the experiments for each single process flow

from A to H. The second experimental set (S2) is designed according to the results obtained in the first experimental set (S1) to analyze the effects of increasing the number of process flows. Two approaches are used to increase the number of process flows. The first approach starts with a process flow which has the shortest CT index in S1, while the second approach starts with a process flow which has the longest CT index in S1. Four experiments under each approach are considered by doubling the number of process flows in each experiment. The third experimental set (S3) has four different mixture combinations of eight main process flows for the comparison reasons. Accordingly, the first mixture represents the equal release percentages, the second product mix is the base case scenario percentages given in Table 2, the third experiment includes the high product mix percentages for the flows having high CT index performance and the last one has the high product mix percentages for the flows having low CT index performance. The percentages in the third and fourth experiments are defined after the first experimental set (S1) results.

6 RESULTS

6.1 Analysis of single flows

The purpose of this experimental set is to characterize the process flows based on their CT index performances and their effects on the photolithography tool sets. The results of the experiments are given in Figure 3 and in Figure 4. Figure 3 shows that process flows having CT index performance from minimum to maximum are D, B, C, H, E, A, F and G. Not surprisingly, it is observed that most single process flows represent parallel results with the variation given in Table 1 in the input analysis section 4. To illustrate, process flow D has the minimum cycle time index and variation. Also, the process flows F and G have the maximum performance and variation. In addition, a similar relationship is obtained with the number of passes given in Table 2 in section 5. Process flows G, F and A which have high number of passes show high CT index performances. However, process flows C and E don't show this relationship. Although process flow C has the maximum number of passes, it has the third lowest CT index performance. Likewise, process flow E has the minimum number of passes but its CT index performance is higher than process flows B, C and D.

Figure 4 and Table 5 represent the results of tool utilizations and tool wait times in the photolithography area under each single process flow. According to the results, process flows E and H show highly imbalanced tool utilizations, whereas process flow C utilizes all the tools almost at full capacity. Likewise, process flow G has similar behaviour except for tools 3 and 4. In addition, process flows B and D show similar results with slightly different values like process flows A and F.



Figure 3: Simulated CT index performance of single flows.



Figure 4: Tool utilizations under each single process flow.

Imbalanced tool utilizations are the result of the different tool capability profiles of the processes. Some of the tools have a higher percentage of capabilities under each process flow as shown in Table 4. With regard to tool wait times, high utilizations represent higher wait times. The process flows such as process flows C and G utilize the tools almost at full capacity and they have the longest wait times due to high tool utilizations. Also, process flows E and H shows the smallest wait times less than one minute for Tool 3 and 4. Process flows D, B and F have the relatively balanced wait times over the tools compared to the other flows.

Table 5: Simulated tool wait times (mins) (S1).

Tool Wait Time (Min) (S1)					
Flows	Tool 1	Tool 2	Tool 3	Tool 4	Tool 5
А	23.11	26.08	21.84	56.94	26.57
В	4.34	4.50	4.14	7.84	4.87
С	793.83	791.53	806.01	799.02	798.33
D	2.97	3.49	7.50	7.26	3.91
Е	10.74	12.42	0.11	0.42	12.17
F	10.17	10.94	10.96	14.84	11.88
G	921.28	915.21	13.62	19.02	919.20
Н	20.08	21.99	0.17	0.59	21.73

6.2 The impact of increasing product diversity

Product diversity was investigated by increasing the number of process flows in the fab. Two approaches were used to increase the number of process flows while keeping total wafer start volumes constant. Each approach has a set of

four experiments given in Table 6 and the number of process flows are doubled. The first approach starts with the process flow which has the minimum CT index performance, while the second approach starts with the process flow which has the maximum CT index performance. The rationale behind selecting the two processes with extreme CT index performance measures was to show the effect of increasing process diversity. The results of the first experimental set show that the first four process flows having the minimum CT index performance are the process flows D, B, C and H. Accordingly, the number of process flows for the first approach are increased by first selecting the process flow D in the first experiment, then D and B in the second experiment, D, B, C and H in the third experiment Y3. As for the last experiment, all of the process flows under equal wafer starts are considered. In the same way, the number of process flows are increased in the second approach.

Table 6: Experiments under two approaches (S2).

	First	Second	
	Approach	Approach	
Experiment	Short to Long	Long to Short	
No	CT index	CT index	
1	D	G	
2	D-B	G-F	
3	D-B-C-H	G-F-A-E	
4	All	All	

Figure 5 compares the effects of increasing the number of process flows under both approaches. It is observed that increasing the number of process flows results in a gradual increase in CT index performances under the first approach, whereas it results in a gradual decrease in performances under the second approach. As new process flows having higher CT index performance are introduced in the first approach, the effect of the processes with low CT indices is diluted, and higher overall CT index performance is observed. However, the dilution effect of the processes with high CT indices in the second approach decreases the overall CT index performance.



Figure 5: Dilution effect on overall CT index performance.



Figure 6: Percentage changes in CT index performance of process flows under Pattern 1.

In addition, the CT index performances of process flows under both approaches are compared to their single process flow performances and the changes in percentages are depicted in Figure 6 for the first approach. According to the results, as the mix changes, process flows C and G are effected significantly and dramatic reductions over 17 % and 10 % in their CT index performances are observed in Figure 6 respectively. The same results are obtained also in the second approach. The reason is considered to be that process flows C and G are characteristic of process flows that are not mature where alternative paths may not be in place.

Further, the relationship between increasing the number of process flows and tool utilizations under both approaches are examined in Figure 7 and Figure 8. As the number of process flows increase in the first approach, all the tool utilizations increase in Figure 7 except for Tool 3. Tool 3 represents almost equal tool utilization values and it is not sensitive to the product mix changes. As the mix increases in favor of longer processes there is a greater loading on photolithography tools. However, as the mix changes toward fewer photolithography passes in the second approach, generally tool utilizations reduce in Figure 8 except for the first scenario at Tools 3 and 4.



Figure 7: Changes in tool utilizations (Pattern 1).

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Figure 8: Changes in tool utilizations (Pattern 2).

6.3 Analysis of multiple flows

The simulation model was then used to explore CT effects where the starting volumes are changed while keeping the total starts quantity constant. The first product mix scenario (M1) considers equal release rates for all process flows, the second one (M2) is the base case scenario given in Table 2, the third scenario (M3) assigns high release rates to the process flows which have high CT index performances in decreasing manner, and for the last product mix scenario (M4) assigns high release rates to the process flows which have low CT index performances.

Table 7: Percentages (%) of process flows under each scenario (S3).

Flows	M1	M2	M3	M4
A	12.5	17.5	17.5	7.5
В	12.5	17.5	5.0	20.0
С	12.5	17.5	7.5	17.5
D	12.5	12.5	2.5	22.5
Е	12.5	12.5	15.0	10.0
F	12.5	12.5	20.0	5.0
G	12.5	5.0	22.5	2.5
Н	12.5	5.0	10.0	15.0

Figure 9 represents overall CT index performances of the product mix scenarios. According to the results, M1 and M2 represent close performance values, however, M3 results in the highest CT index performance. Also M4 represents the lowest CT index performance under all the scenarios. The reason is that process flows having high CT index performance values cause higher effect on overall performance in M3, but in scenario M4 this effect is minimal. In short, it can be concluded that overall CT index performance is directly proportional to the release volumes of process flows.

The percentage changes in the CT index performances of process flows are compared to the single flow situations as shown in Figure 10. Similar to the previous experimental set (S2), process flows C and G are affected significantly under multi-flow scenarios. In process flow C, the percentage



Figure 9: Performance results under different product scenarios.

change in the CT index performance is about 18 % but it is not sensitive to the different release volumes. Process flow G shows significant performance changes under different release volumes.



Figure 10: Percentage changes in CT index performance of process flows under different product mix scenarios.

The results of tool utilizations and tool wait times are given in Figure 11 and in Figure 12. Tool 1 and Tool 2 represent higher tool utilization values compared to the other tools. Also, Tool 3, Tool 4 and Tool 5 have close utilization values. However unlike the utilization values, Tool 4 and Tool 5 show longer wait times, especially Tool 4 under base scenario (M2) has the longest wait time. Since high wait times may show that more effective dispatching policies are needed to reduce disproportioned wait times.



Figure 11: Tool utilizations under different product mix scenarios.



Figure 12: Tool wait times under different product mix scenarios.

7 CONCLUDING REMARKS

In this study, the effects of single and multiple flows in a medium level ASIC fab are examined by a simple fab simulation model. Significant preliminary work was performed before the simulation coding phase. This preliminary work included the conceptual model design, data gathering, data manipulation and preparation for input data analysis. Fab data was analyzed to examine the behaviour of cycle time in a situation where product and volume diversity was present. A simulation model was developed to evaluate single process flows, increasing multiple process flows in equal volumes and multiple process flows in different volumes. The photolithography area was looked at in greater detail to explore equipment utilization effects.

A number of conclusions can be drawn from the experimental results: (1) each process flow has a unique cycle time index performance; 2) each process flow has a tool utilization characteristic on photolithography tools, because of capability/recipe/ tool profiles and the numbers of passes of the process; (3) different release volumes on a mix of process flows that keeps the total release volumes constant affects the photolithography area performances and hence the overall cycle time index and (4) some of the process flows are more sensitive to different release rates than others.

It is important to note that batching policies and batch machines have a significant impact on the fab performance under a given product mix Akcali et al. (2000). The model described here is not sophisticated enough to capture these impacts. Although the model represents the impacts of multiple process flows on the photolithography area, we assume that the overall CT index performance and CT index performance of process flows will have larger deviations with the cycle time performance under detailed full fab models as discussed in the studies of Rose (2000) and Rose (2007).

A further research direction can be the analysis of the process flows under different loading levels under stochastic processing times and finding the optimum levels of product mix for a stable fab performance.

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REFERENCES

- Akcali, E., K. Nemoto, and R. Uzsoy. 2001. Cycle-time improvements for photolithography process in semiconductor manufacturing. *IEEE Transactions on Semiconductor Manufacturing* 14 (1): 48–56.
- Akcali, E., D. G. Uzsoy, R.and Hiscock, A. L. Moser, and T. J. Teyner. 2000. Alternative loading and dispatching policies for furnace operations in semiconductor manufacturing: A comparison by simulation. In *Proceedings* of the 2000 Winter Simulation Conference, 1428–1435.
- Dummler, M. A. 2000. Analysis of the instationary behavior of a wafer fab during product mix changes. In *Proceedings of the 2000 Winter Simulation Conference*, 1436–1442.
- Iwata, Y., and S. C. Wood. 2000. Effect of fab scale, process diversity and setup on semiconductor wafer processing cost. In Proc. IEEE/SEMI Advanced Semiconductor Manufacturing Conference, 237–244.
- Monch, L., M. Prause, and V. Schmalfass. 2001. Simulationbased solution of load-balancing problems in the photolithography area of a semiconductor wafer fabrication facility. In *Proceedings of the 2001 Winter Simulation Conference*, 1170–1177.
- Nayani, N., and M. Mollaghasemi. 1998. Validation and verification of the simulation model of a photolithography process in semiconductor manufacturing. In *Proceedings of the 1998 Winter Simulation Conference*, 1017–1022.
- Neacy, E., N. Abt, S. Brown, M. McDavid, J. Robinson, S. Srodes, and T. Stanley. 1993. Cost analysis for a multiple product / multiple process factory: Application of sematech's future factory design methodology. In *IEEE/SEMI Advanced Semiconductor Manufacturing Conference*, 212–219.
- Park, S., J. Fowler, M. Carlyle, and M. Hickie. 1999. Assessment of potential gains in productivity due to proactive reticle management using discrete event simulation. In *Proceedings of the 1999 Winter Simulation Conference*, 856–864.
- Peikert, A., J. Thoma, and S. Brown. 1998. A rapid modeling technique for measurable improvements in factory performance. In *Proceedings of the 1998 Winter Simulation Conference*, 1011–1015.
- Robinson, S. 2006. Conceptual modeling for simulation: issues and research requirements. In *Proceedings of* the 2006 Winter Simulation Conference, 792–800.

- Rose, O. 2000. Why do simple wafer fab models fail in certain scenarios? In *Proceedings of the 2000 Winter Simulation Conference*, 1481–1490.
- Rose, O. 2007. Improved simple simulation models for semiconductor wafer factories. In *Proceedings of the* 1998 Winter Simulation Conference, 1708–1712.
- Spence, A., and D. Welter. 1987. Capacity planning of a photolithography work cell in a wafer manufacturing line. In *Proc. IEEE Conf. Robotics and Automation*, 702–708.

Tecnomatix 2007. <http://www.ugs.com>.

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