SIMULATION ANALYSIS OF CLUSTER TOOL OPERATIONS IN WAFER FABRICATION

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ABSTRACT

Cluster tools have been one of the proposed alternatives to improve operations performance in semiconductor fabrication. The benefits include high yield throughput, less contamination and less human involvement. Perkinson et al. (1994, 1996) developed analytical models to predict the minimum theoretical time required to complete the cycle in a cluster tool. This paper addresses the verification of these analytical models using simulation. Two simulation models were developed – one with simple configuration and another one that incorporates parallel chambers. The implementation of parallel chambers for the longest process in the cluster tool is tested as the potential area of performance improvement.

1 INTRODUCTION

A cluster tool is an integrated tool which combines several subsequent steps of semiconductor manufacturing, for example, during the lithography stage which consists of coating, exposure and development processes. A cluster tool comprises several single-wafer processing modules, namely loadlocks, processing chambers and transporter. These three modules can be in different configurations such as single or multiple loadlocks for loading and unloading; serial, parallel or mixed processing chambers, and single or double robotic arms for transportation of wafers within the cluster tool. The benefits of this integrated tool include reduction of manual handling (and thus less contamination) as well as reduction of capital and floor space. Besides that, processing of wafers in cluster tools is pipelined and thus the cycle time is reduced compared to the conventional approach of using consecutive machines (Niedermayer and Rose 2004).

However, the challenge for cluster tools lies in its complex behavior. The variation of lot cycle time is highly dependent on the situation inside the cluster tool during processing. When a cluster tool processes lots in parallel, each lot overlaps with other lots. Thus, the lot cycle time depends considerably on the lot combinations inside the cluster tool (Niedermayer and Rose 2004). For the past decade, the implementation of cluster tool in semiconductor industry has gradually been developed to obtain higher throughput and to reduce cycle time in fabs.

To predict the minimum theoretical time required to complete the cycle in cluster tool, Perkinson, Gyurcsik, and McLarty (1994) developed an analytical model. This analytical model is derived for simple series configuration of cluster tool, whereas Perkinson et al. (1996) presented the analytical model of a more complex configuration of cluster tool such as the implementation of parallel chambers, the use of loadlock as a queue, etc. However, Perkinson, Gyurcsik, and McLarty (1994, 1996) have not shown any simulation verification of the results obtained from the analytical models. In this paper, the first objective is to verify the accuracy of the analytical models, whereas the second objective is to achieve the percentage of improvement when parallel chambers are incorporated in the cluster tool. Two simulation models are developed using AutoMod software (Brooks Automation 2005). The first model is built with a simple configuration and the purpose is solely to observe the behavior based on the analytical model. The second model is built with the incorporation of parallel chambers in the longest processing chamber in order to verify the potential areas of performance improvement in cluster tools.

2 ANALYTICAL MODEL 1 (PERKINSON ET AL., 1994)

Perkinson, Gyurcsik, and McLarty (1994) presented a steady state as well as a transient state analysis of the relationship between process time, transport time and maximum throughput in the cluster tool process. They developed analytical results in terms of fundamental period (FP) which is defined as the time difference between subsequent completed wafers arriving at the loadlock before exiting the cluster tool. In this analysis, the following variables are used:

N = number of process chambers, P = process time of a chamber, T = transport time between chambers, FP = fundamental period of the tool, T_{load} = loading time of cluster, T_{unload} = unloading time of cluster, NW = number of wafers in the lot.

2.1 Steady State Analysis

In cluster tool operations, two kinds of constraints can exist namely transport constraint and process constraint. Transport constraint is the situation when the transporter is always busy, i.e., when a processing chamber completes the processing of a wafer, it has to wait for the transporter in order to unload the finished wafer. Perkinson, Gyurcsik, and McLarty (1994) showed that in transport constraint, the fundamental period is a function of the transport time (T) and number of chambers (N), and is independent of process time (P). In the other situation, the transporter may sometimes be idle and so in this case the transporter has to wait for the processing chamber to finish its operation. This is called as process constraint and in this the fundamental period is determined by process time and transport time and is independent of number of chambers (Perkinson, Gyurcsik, and McLarty 1994).

Transport constraint:	FP = 2 T (N+1)	(1a)
Process constraint:	FP = P + 4 T	(1b)

Thus, in transport constraint the variation of process time will not affect FP value, while in process constraint only the slowest process (longest process time) will affect the FP value. The type of constraint in which a cluster tool operates only depends on the relationship between the number of chambers and the process time to transport time ratio (P/T). If P/T < 2(N-1) then the transport constraint applies, otherwise if P/T > 2(N-1) then the process constraint applies.

2.2 Transient State Analysis

A complete description of cluster tool performance accounts for the transient effects of initiating and terminating the processing of a lot of wafers. Therefore, the time per lot (TL) is determined by the steady state time per wafer (FP) multiplied by the number of wafers in the lot (NW) added to the transient effect.

$$TL = NW * FP + \text{transient.}$$
 (2)

Perkinson, Gyurcsik, and McLarty (1994) modeled the transient period as the sum of times for cluster loading (T_{load}) , transition A (from first wafer to the steady state), transition B (from steady state to the last wafer) and cluster unloading (T_{unload}) minus the fundamental period multiplied by (N-I). Transition A and transition B are modeled by the following set of equations:

Transition A =
$$\sum_{K=1}^{Z} P + 2T + \sum_{K=Z+1}^{N-1} 2KT$$
(3)
where Z = min $\left[N - 1, INT \left(\frac{P}{T} + 2 \right) \right]$
Transition B =
$$\sum_{K=1}^{Z} P + 4T + \sum_{K=Z+1}^{N-1} 2(K+1)T - 3T$$
(4)

If Z in the equation assumes the value N-1, the cluster tool remains in process constraint throughout the processing of a lot. When Z is defined by P/T, Z represents the maximum number of chambers that can be in use before the cluster tool enters the transport constraint. The sum of transition A and transition B can be expressed as follows:

$$2(N-1)(P+4T) - T(2N+1), \text{ if } Z = N-1$$
(5a)

$$2Z(P+3T) - 2T(Z+1)^2 - T, \text{ if } Z = INT\left(\frac{\frac{P}{T}+2}{2}\right)$$
 (5b)

The complete model of time per lot is given as:

$$TL = NW * FP + T_{load} + \text{transition A} + \text{transition B} + T_{unload} - (N-1)FP$$
(6)

2.3 Simulation Setup

Model 1 as presented in Figure 1 is a simple fourchamber cluster tool with two loadlocks and one robotic arm as transporter. Each of the single-wafer chambers has different processes. This model does not include parallel chambers. One lot of 25 wafers enters the system and pumped to vacuum in loadlock1. Subsequently, one piece of wafer will be transported from loadlock1 to the next chamber until the last piece of wafer. At loadlock2, wafers are accumulated into a lot before finally vented to the ambient pressure and transferred out of the system.



Figure 1: Illustration of Model 1

The setup of model 1 is as follows:

• In setting the transport time (*T*), the time for wafer pick up, retraction, rotation to the next chamber, expansion

and wafer delivery sum up to approximately 12 seconds. The transport time is taken as a deterministic constant of 12 seconds.

- For transport time (*T*) of 12 seconds and four chambers (N = 4), the critical value of process time (*P*) at which the type of constraint changes is equal to 72 seconds. Therefore, the process time (*P*) is varied deterministically at an interval of 10 seconds in such a way that six values fall in the transport constraint (20, 30, 40, 50, 60, 70 seconds) and six values in the process constraint (80, 90, 100, 110, 120, 130 seconds).
- One lot of wafers is pumped down to vacuum once entering cluster tool in loadlock1. The time for pumping (T_{load}) is a deterministic constant of 5 seconds
- One lot of wafers is vented up to atmospheric pressure before exiting cluster tool in loadlock2. The time for venting (T_{unload}) is a deterministic constant of 5 seconds
- Breakdown and failure of components are not considered.
- Model is run only once in the simulation since deterministic constants are used as input

2.4 Results of Simulation Model 1:

Table 1 shows the result when the process time is varied from 20 to 130 seconds. The FP values are recorded for the first five wafers exiting the cluster. Theoretical FP values are calculated using equation (1a) for the transport constraint and equation (1b) for the process constraint. Table 2 shows the comparison between the theoretical and simulated results for the cycle time of one lot of wafers. Theoretical TL is calculated based on equation (6). Difference in percentage in Table 2 is calculated with the formula (Simulated TL – Theoretical TL)/ Theoretical TL.

From the simulation results shown in Table 1, it is observed that the transition period from transport constraint to process constraint occurs at process time in between 60 to 70 seconds. When processing time varied from 20 to 60 seconds, FP value is constant at 120 (theoretical) and 109 (simulated). This value shows that at this range, the cluster system is in transport constraint where the variation in process time does not affect the FP value. Further, from process time = 70 seconds onwards, as the process time is increased, both theoretical and simulated FP values increase as well. This observation shows that from P = 70 seconds onwards, the system is in process constraint where variation in process time affects the FP value. In process constraint, FP value is determined by the longest process time in the system. From Table 2 the maximum difference between theoretical and simulated TL value is 13.36% which occurs at P = 20 seconds. This difference decreases with the increase in the process time. Figure 2 illustrates the comparison between theoretical and simulated FP/P values.

From Figure 2, it can be observed that the difference between theoretical and simulated FP/P values is maximum at P = 20 seconds. With the increase in process time (P), the difference between theoretical and simulated FP/P values goes on decreasing and finally the theoretical FP/P value approaches the simulated FP/P value.



Figure 2: Performance curves of simulation results

		Deterministic Process Time (P) in Region 1 (sec)					1 (sec)	Deterministic Process Time (P) in Region 2 (sec			(sec)		
Wafer No.	Results	20	30	40	50	60	70	80	90	100	110	120	130
1 st	Th. FP Sim. FP	1 <u>20</u> 109	120 109		1 <u>20</u> 109	120 109	120 115.5	1 <u>28</u> 125.5	<u>138</u> 135.5	148 145.5	1 <u>58</u> 155.5	168 165.5	<u>178</u> 175.5
2 nd	Th. FP	120	120	120	120	120	120	128	138	148	158	168	178
-	Sim. FP	109	109	109	109	109	114	124	134	144	154	164	174
3 rd	Th. FP	120	120	120	120	120	120	128	138	148	158	168	178
Ŭ	Sim. FP	109	109	109	109	109	114	124	134	144	154	164	174
4 th	Th. FP	120	120	120	120	120	120	128	138	148	158	168	178
	Sim FP	109	109	109	109	109	114	124	134	144	154	164	174
5 th	Th. FP	120	120	120	120	120	120	128	138	148	158	168	178
Ŭ	Sim. FP	109	109	109	109	109	114	124	134	144	154	164	174

Table 1: Results for theoretical vs. simulated FP

Process Time (s)	Th. FP (s)	Th. TL (s)	Sim. TL (s)	Difference (%)
20	120	2654	3008.61	13.36
30	120	2686	3009.91	12.06
40	120	2726	3011.24	10.46
50	120	3130	3012.98	-3.74
60	120	3190	3009.98	-5.64
70	120	3250	3144.73	-3.24
80	128	3486	3424.38	-1.77
90	138	3766	3704.16	-1.64
100	148	4046	3983.90	-1.54
110	158	4326	4263.90	-1.44
120	168	4606	4543.59	-1.36
130	178	4886	4823.21	-1.29

Table 2: Theoretical vs simulated time per lot (TL)

The differences between theoretical and simulated TL values can be explained by the setting of the robotic arm which determines the transport time. In theoretical calculation, the transport time is taken as a deterministic constant of 12 seconds. However, the transport time is dependent on the difference in rotation angle between the chambers. The setting of total 12 seconds of transport time is only from one chamber to the next neighbor chamber and not the next two chambers. Therefore, although rotational speed has been set to consume the least portion of 12 seconds, nevertheless the variation in actual value of transport time is unavoidable. However, the difference of theoretical and simulated value is still within the acceptable range, thus verifying the accuracy of the analytical model developed by Perkinson, Gyurcsik, and McLarty (1994).

3 ANALYTICAL MODEL 2 (PERKINSON, GYURCSIK, AND MCLARTY 1996)

Perkinson, Gyurcsik, and McLarty (1996) presented a steady state analysis of the cluster tool behavior when parallel identical chambers are incorporated. Figure 3 gives an overview of model 2. For model 2, the analysis presented only the process constraint because the process time affects the throughput only in the process constraint.

3.1 Steady State Analysis

The additional notations used are:

- P_{id} = Deterministic process time where identical (cooling) chambers are implemented
- P_{eff} = Effective process time of the identical chambers
- N_{id} = Number of identical chambers

FP_{id} = Fundamental period of the cluster tool with identical chambers

Perkinson, Gyurcsik, and McLarty (1996) examined the effects of incorporating identical chambers on the throughput of the cluster tool using a graphical approach.



Figure 3: Illustration of model 2

This work focused on clusters operating in the process constrained region because the process times affect throughput only in the process constrained region; throughput in the transport constrained region is independent of process times. The ultimate purpose of this development is to determine the process time of an individual chamber that has the same net effect on the performance of the cluster as the N_{id} identical chambers. Perkinson, Gyurcsik, and McLarty (1996) established the following relationship:

$$P_{\rm id} = N_{id} \times (P + 4T) - 4T \tag{7}$$

In (7), the original process time of the individual chambers (P) must be the effective process time of the identical chambers P_{eff} . Substituting P_{eff} for P in (7) and solving for P_{eff} yields the following equation:

$$P_{eff} = \frac{P_{id} + 4T}{N_{id}} - 4T \tag{8}$$

where N_{id} is the number of identical chambers and P_{id} is the process length of the identical chambers. In this model, N_{id} identical chambers with process length P_{id} have the same average effect on the cluster tool as one chamber with process length P_{eff} .

In the analysis of model 1, the throughput and fundamental period is determined by the longest process time. Thus, if P_{eff} being the longest process in the cluster, then the formulation for the fundamental period is as follows:

$$FP = P_{id} + 4T$$

$$FP_{id} = P_{eff} + 4T$$
(9)

where FP is the fundamental period of the cluster tool without the incorporation of identical chambers and FP_{id} is fundamental period of the cluster tool with Nid identical chambers.

3.2 Simulation Setup

Model 2 is based on the deposition process in the semiconductor wafer fabrication. It consists of 2 loadlocks, 4 serial deposition chambers and 8 parallel cooling chambers as presented in Figure 3. The beginning of the cycle starts from venting up of loadlock1 to reach atmospheric pressure. Subsequently, door at loadlock1 is opened to allow one lot of wafers to enter the system. Door is then closed and loadlock1 is brought down to vacuum. Then, one piece of wafer is transferred to the first chamber (deposition chamber 1) and subsequently to the second, third, and fourth chambers before finally it goes into one of the parallel chambers for cooling process. After this, the door at loadlock2 (at vacuum) will open and the completed wafer is transferred to loadlock2. When one lot of wafers had entered loadlock2, the loadlock2 is vented up to atmospheric pressure before finally the lot exits the system.

Table 3 shows the real data values from a semiconductor fab. Model 2 is simulated according to the following three setups:

- Setup A: Here, cleaning of deposition chambers is not considered. Also, cooling time (P cooling) is not taken based on Table 3, but as a random variable in order to verify the analytical results of model 2 where parallel cooling chambers are incorporated. The range of P cooling is taken as 400-2000 seconds.
- Setup B: In this setup, model 1 and model 2 are simulated with the input data of Table 3, except that P cooling is assumed to vary in the range of 400-2000 seconds as in setup A.
- Setup C: In this setup, model 2 is simulated with the exact input data of Table 3.

Simulation of model 2 is carried out for 5 snaps, where each snap is counted for 12 hours of real industrial running time. Here, FP and FP_{id} values are calculated based on the cumulative average of the results of the 5 snaps

3.3 **Results of Model 2 with Setup A**

In this setup, deposition chamber cleaning process is not considered and P cooling is varied from 400 to 2000 seconds; while the other input parameters are taken according to Table 3. P cooling is assumed to be the bottleneck of the system (P_{id}) . The simulation results are compared to the theoretical results obtained by equations (7-9). The results for setup A are presented in Table 4 with the theoretical and simulated FP_{id} values as well as the number of parallel chambers involved in the system.

Loading		No. of loadlock	2
	e e	No. of wafers per lot	25
	Operation Availability	Deposition chamber clean cvcle Deposition chamber clean time	3 wafers 170 sec (constant)
	Deposition	No. of chambers Deposition time (P_deposition)	4 (series) 173 sec (triangular)
	Cooling	No. of chambers Cooling time (P_cooling)	8 (parallel) 119 sec (triangular)
	Cooling Transporter	No. of chambers Cooling time (P_cooling) Transport time (T) No. of robot Wafer routing	8 (parallel) 119 sec (triangular) 12 sec (constant) 1 FIFO

Table 3: Industrial input data for model 2

Table 4: Theoretical vs simulated FPid results

Vent time (Tunload)

106 sec

(constant)

Others

P cooling		Theoritical	Simulated
time(s)	N _{id}	FP _{id}	FP _{id}
400	2	224	226.20
600	3	216	224.85
800	4	212	224.20
1000	5	209.6	224.20
1200	6	208	224.59
1400	7	204	225.26
1600	8	206	225.52
1800	8	231	239.32
2000	8	256	259.52



Figure 4: Theoretical vs. simulated FP_{id}/P curves for model 2 with setup A

Using the theoretical and simulated results of FP_{id} from Table 4 and taking transport time (T) to be 12 seconds, FP_{id}/P is plotted against P/T as a graph in Figure 4. Based on Figure 4, the difference between theoretical and simulated FP_{id}/P varies from 1 to 10.21%, which is in the acceptable range of the simulation results. The difference between theoretical and simulated FP_{id}/P can be explained in a similar way to that of simulation model 1, i.e., the variation is due to the setting of robotic arm in rotating from one chamber to another.

3.4 Results of Model 2 with Setup B

Setup B is used to obtain the percentage throughput improvement of model 2 over model 1 with input based on Table 3 except P_cooling varying in the range of 400-2000 seconds. The deposition cleaning cycle is included in this setup. The results for model 1 and model 2, respectively, are shown in Table 5 and Table 6.

In this setup, the characteristic of model 1 and model 2 are observed when the process time of one chamber is longer than the process time of other chambers. In model 1 (without having parallel chambers) considering the fourth chamber with the longest process time, chamber 3 will become choked up. This will greatly affect the throughput and cycle time. The incorporation of parallel chambers at the longest process in model 2 will positively affect the throughput and cycle time. From the results obtained in Table 5 and Table 6, the percentage of improvement is calculated and shown in Table 7.

From Table 7, it can be observed that the improvement of cycle time for each increment of 200 seconds in P cooling is subsequently 14.76%, 7.59%, 4.62%, 3.31%, 2.25%, 1.65%, 1.27%, and 0.91%. The percentage of improvement reduces as P cooling is increased. Similarly, the improvement in throughput is 66.07%, 67.37%, 71%, 69.74%, 60.71%, 81.79%, 48.86%, and 59.14%. The maximum improvement of results in the above table occurs at P cooling = 2000 seconds where result of model 2, namely cycle time is reduced by 61.42%, throughput is increased by 595.5%, and fundamental period is reduced by 86.16% compared to the results of model 1. Note that when P cooling time is less than 1600 seconds, the system does not use all the available number of parallel chambers. With the increase of 200 seconds in P cooling, the number of chambers used increases by one until the maximum value of 8 chambers. These results clearly show that performance of cluster tools could be improved with incorporating identical chambers for the longest process.

3.5 Results of Model 2 with Setup C

Setup C takes the exact input data of Table 3. From the data, the total process time at loadlock2 is 125 (pump time) + 106 (vent time) = 231 sec. Since P_deposition = 173 seconds and P_cooling = 119 seconds, loadlock2 acts as the longest process time and becomes the bottleneck process. Still the parallel chambers are incorporated for cool-

ing process. These parallel chambers have dual functions, namely to carry out the cooling process as well as to be the queue for wafers since bottleneck process is at loadlock2. By doing this, process would be able to flow continuously. The results of cycle time, time per lot, throughput and simulated FP are presented in Table 8.

P_cooli ng (s)	Cycle time (s)	Time per Lot (s)	Through- put (wafers)	Simu- lated FP (s)
400	1774.29	13684.16	85	496
600	2544.72	18840.00	61	695
800	3303.02	23245.49	47	895
1000	4053.53	28245.49	38	1043
1200	4792.56	33245.49	32	1293
1400	5525.04	38245.49	28	1495
1600	6218.71	-	24	1691
1800	6936.27	-	22	1999
2000	7629.35	-	20	2092

Table 5: Performance of model 1 with setup B

Table 6: Performance of model 2 with setup B

Tuble C	ruble 0. I erformance of model 2 with setup D							
P_cool	Cycle	Time	Throughput	Simu-				
ing (s)	time (s)	per Lot	(wafers)	lated				
		(s)		FP (s)				
400	1329.61	8241.25	145	288.09				
600	1531.39	8443.22	144	288.11				
800	1737.19	8664.68	143	289.22				
1000	1944.32	8976.95	143	289.99				
1200	2140.31	9137.30	142	288.93				
1400	2343.12	9361.46	142	289.37				
1600	2534.63	9428.43	141	288.90				
1800	2739.05	9651.13	140	290.67				
2000	2943.61	9895.52	139	289.54				

Table 7: Performance comparison of model 2 over model 1 with setup B

Longest process time (s)	N _{id} for model 2	Cycle time (%)	Throughput (%)	FP (%)
400	2	-25.06	70.82	-41.89
600	3	-39.82	136.89	-58.54
800	4	-47.41	204.26	-67.68
1000	5	-52.03	275.26	-72.20
1200	6	-55.34	345.00	-77.66
1400	7	-57.59	405.71	-80.64
1600	8	-59.24	487.50	-82.91
1800	8	-60.51	536.36	-85.46
2000	8	-61.42	595.50	-86.16

Table 8: Performance of model 2 with setup C

P_cooling	Cycle	Time per	Throughput	Simulated		
time (s)	time (s)	lot (s)	(wafers)	FP (s)		
119	1056.93	8216.06	146	290.54		

In model 2 with setups B & C, cleaning of deposition chambers is considered with clean time of 170 seconds and a clean cycle of 3 wafers per clean cycle. For this kind of set up, the analytical results have not been established yet. That's why in these cases only simulated results have been presented.

4 CONCLUSION

Previous research has clearly shown the analytical models to predict the behavior of cluster tool. In this paper, simulation model is built to verify the results of analytical models. This paper also presents the comparison of performance when cluster tool is run with and without parallel chambers. The percentage of improvement in the implementation of parallel chambers is expected to provide useful input during the cluster tool investment decision process where the percentage of improvement is compared to the trade-off in adding chambers. Two simulation models are built. First model represents simple cluster tool with a purpose to verify the analytical model derived by previous research. The second model includes cluster tool incorporated with parallel chambers.

REFERENCES

Brooks Automation, Inc. 2005. Automod User's Manual

- Niedermayer H., and O. Rose. 2004. A Simulation-based Analysis of the Cycle Time of Cluster Tools in Semiconductor Manufacturing. In *Proceedings of the Annual IIE Industrial Engineering Research Conference*, Houston, Texas.
- Perkinson T. L., R. S. Gyurcsik, and P. K. McLarty. 1996. Single-Wafer Cluster Tool Performance: An Analysis of the Effects of Redundant Chambers and Revisitation Sequences on Throughput. *IEEE Transaction on Semiconductor Manufacturing*, 9(3):384-400.
- Perkinson, T. L., P. K. McLarty, R. S. Gyurcsik and R. K. III. Cavin. 1994. Single-wafer cluster tool performance: An analysis of throughput. *IEEE Transactions* on Semiconductor Manufacturing, 7(3):369-373.

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