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ASAP APPLICATIONS OF SIMULATION MODELING IN A WAFER FAB

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ABSTRACT

The authors define 4 levels of complexity in simulation modeling. The ability of the models to predict bottlenecks in the fab, Capability of the model to be used for strategic applications such as cycle time reduction, Simulate complex dispatch rules using the model, Capability of the model to predict operational output of the wafer fab that is clean room outs by product by day. This paper presents the operational applications of the ASAP simulation model to provide wip flush to the test probe area and the flush provided to planning for financial estimates and fab commitments. WIP flush is defined as a prediction of the fab output by device/technology by day. In general the ability to predict the shorter the time horizon the more difficult it is to predict the output accurately. Excursions are defined as any deviations in the normal processing of wafers such as unusually high particles being shown on Statistical Process Control charts etc.

1 INTRODUCTION

A comprehensive simulation model in AutoSched AP was developed at DMOS 5 (An 8" wafer fab at Texas Instruments).The simulation model encompasses all the major inputs such as process flows, devices, tools, PM's, wafer qualification, engineering flows, wip profile of the shop floor. The data inputs were collected and the model output was validated over a span of 1 year. The model was validated by comparing the model output with actuals in wafer outs, cycle time and utilization of key tools. Keeping the information updated in the model is an extremely important task and entails a huge effort from the IE group.

1.1 ASAP Inputs/Outputs

The routing and part information is captured from the MES system using an internally developed central data warehouse. The wip snapshot is captured from the MES system and converted into "order.txt" for the simulation model with the help of VB macros. The planning group provides information on estimates of the projected wafer starts into the factory.

1.1.1 Fab Data Collection

The model consists of about 350-400 devices and 75-100 routes. The process flow routings were extracted from TI's internally developed shop floor control system called SMS. The theoretical process times and throughput rates for each tool and all the recipes was collected by conducting time studies. Each recipe in the fab was timed to determine the exact throughput and consideration was given to the 4 main tool types modeled in ASAP simulation: Batch, Batch Sequential, Serial, Part Sequential. Statistics were collected for Scheduled and Unscheduled Downtime through various reports and manual data collection. The fab data collection process was accomplished in 2 quarters. Scheduled Downtime consists of Qualifications that are based on time or the number of wafers processed. The Qualification information in the model was based on the time studies done by observing the quals actually being performed inside of the fab. PM's were determined based on the logout time from the shop floor control system and cross checking with the engineering technicians. Daily and Weekly PM's were timed. Capability was developed to automatically download the snapshots of WIP in the line and uploading them into the model.

1.1.2 Model Validation

After the initial verification and testing a full quarter was spent validating the simulation output on cycle time, bottleneck tool utilization, wafer outs and moves by tool group by comparing with the reality. In addition this time was used to "duplicate history" by using all the required model inputs and validating to ensure that the model was able to duplicate the outs/cycle time when the inputs were identical to the past inputs. Model output was reviewed with Manufacturing Manager and Module managers for

accuracy and buy-in. The model predicted the CT and outs accurately. This validation process is currently automated.

2 SIMULATION PROJECT APPROACH

A cross-functional team consisting of the module managers was formed to review the model input/output and provide feedback. The output statistics and inputs were reviewed for their specific areas on a regular basis to ensure accuracy and obtain early buy-in.

2.1 Cycle Time Reduction

In Q3'01 TI launched a worldwide fab cycletime reduction initiative to achieve 2 days/mask layer and that meant a cycle time reduction of almost 46% for DMOS5. A cycletime reduction meeting was started involving all the fab management with the Industrial Engineering Manager as the coordinator. All the modules (Photo, Thinfilms, Plasma, CMP, Diffusion) were asked to identify the highest leverage projects for achieving lower cycle time in their respective areas. The entire management met on a weekly basis to develop cycle time projects and review the progress

3 WIPFLUSH USING THE SIMULATION MODEL

In wafer fab manufacturing, test area is one of the bottlenecks. This is due to the fact that the test times are normally very high and secondly the excursions in the line disrupt the streamline flow of the material and as a result at there may be a bubble of inventory reaching the test area. It therefore becomes imperative to be able to predict the incoming wip to better prepare for the Test capacity.

Using simulation model to predict the movement of the wafers through the clean room and the flush to the Test Probe requires a very high level of accuracy in modeling. Few prerequisites to enhance model's accuracy are:

- Providing the state of the tools at the start of the simulation run. Whether they were up or down, and if down how long they have been down and what is the estimated time to bring the tool back up if the tool is hard down.
- On some of the high process time tools, it is important to specify how much of the process time is remaining on the lot that is being processed at the start of the simulation run. If this is not specified then at the start of the simulation run the lot processing on the tool would be start processing from the beginning. This would skew the results of the flush for long process time tools.
- For the lots put on hold, for whatever reason, it is best to leave them on hold for the entire period of run unless the information is available as to when the lots will be released from hold.

An important point to note is that the projected wafer starts loaded in the model are normally not very accurate, this however does not affect the model if the flush is for the time period less than the cycle time of the fastest running device. However, the importance of a fairly accurate projected wafer loadings cannot be undermined as it affects the movement of the wafers in the line.

3.1 Validation of the WIP Flush

The WIP flush example shown in Figure 1 (out of the clean room) from the simulation was validated for 1 quarter before it was used in critical capacity requirements for Test Probe. It was also noticed that the accuracy of the flush dwindles beyond 3 weeks of projections. This time period however would change if there were a major excursion in the line after the flush is generated.

In the graph above the green curve is the flush projection at the beginning of the quarter, this curve remains the same throughout the quarter to see how the fab did compared to the beginning of the quarter prediction. This curve is also the least accurate and there are various reasons for this, firstly, there is no accurate way of knowing how the wafer loadings are going to look like for the entire quarter. Secondly, there are always excursions (one time occurrences) in the line that can skew the clean room outs. For these reasons, the graph is updated with new projections every week. From the past predictions it has been noticed that the projections are 95% accurate for the first 3 weeks, and then the accuracy begins to drops to 80%.

4 CONCLUSIONS

The use of simulation modeling at DMOS5 wafer fab is a success story of how Industrial Engineering principles helps drive the bottom line productivity increases in the fab resulting in CT reduction, accuracy in probe card planning. Simulation modeling was used for tactical applications effectively.

REFERENCES

Mason, S.J, Potti K, and Krishnaswamy, S 1999. Modeling & Simulation at AMD *Institute for Operations Research and Management Sciences*, Arizona State University, Tempe, Arizona

Potti, K. 1994 Using Simulation to calculate WIP levels in Semiconductor Manufacturing. *Advanced Semiconductor Manufacturing Conference*, Boston.

Potti, K. 1995 TPM in Semiconductor Manufacturing,Operational Modeling Workshop. SEMATECH Manufacturing Methods Council

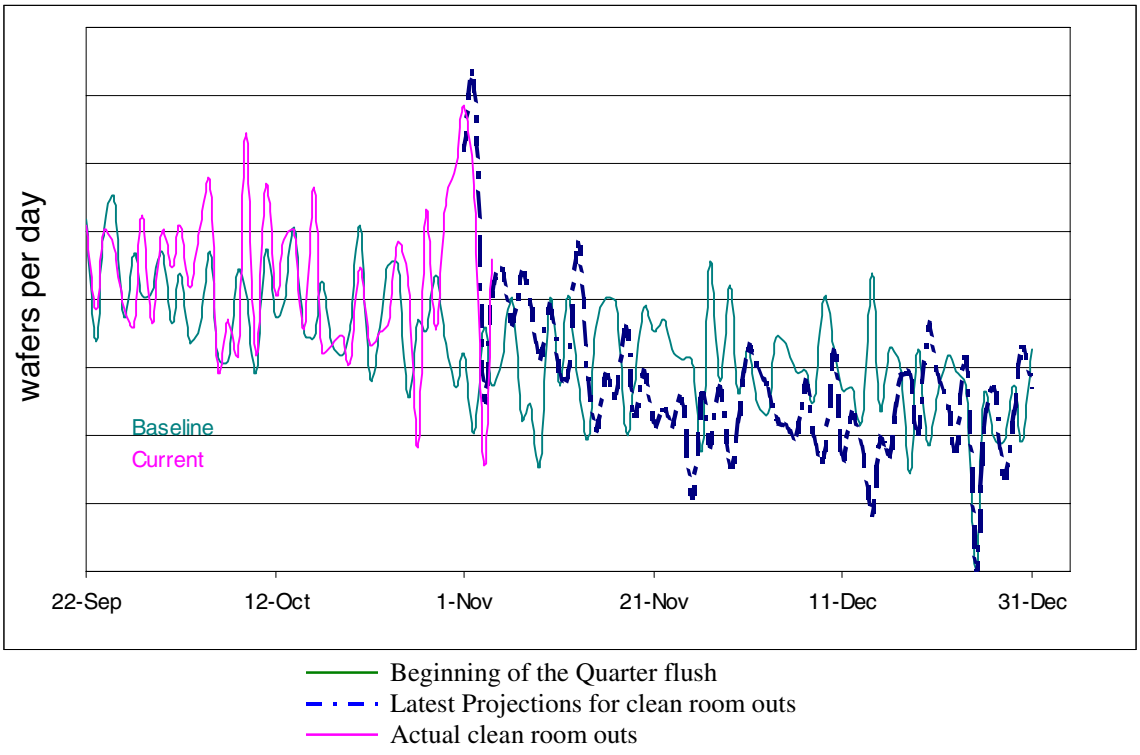

Figure 1: WIP Flush Example

Potti, K and Gupta, Amit 2001. Cycle time Reduction in DMOS5 Wafer Fab at Texas Instruments. *Modeling and Analysis of Semiconductor Manufacturing Conference*

AutoSched AP Version 7.0 Users Manual . Brooks Automation

AUTHOR BIOGRAPHIES

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