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VIRTUAL LIFE ASSESSMENT OF ELECTRONIC HARDWARE USED IN THE ADVANCED AMPHIBIOUS ASSAULT VEHICLE (AAAV)

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ABSTRACT

This paper presents the use of techniques for simulating product qualification as well as for product testing of electronic hardware to be used in the United States Marine Corp's Advanced Amphibious Assault Vehicle. The goal of integrating "up-front" virtual life assessment into the development environment is to increase overall product reliability and decrease overall product cost by decreasing build-test-fix time and promoting optimized tradeoff analysis early in the design stage. Relevant problems included: the positioning of a large microcircuit near the center of the board, weakness to shock loading, and life expectancies of around six (6) to eight (8) years. Failure in the form of electrical opens and/or increased circuit resistance due to thermo-mechanical and random vibration induced fatigue of solder interconnects was predicted as the dominant wearout failure mechanism. A weeklong qualification test is proposed to verify the virtual life assessment results of the life cycle loads.

1 INTRODUCTION

The cost of product ownership in addition to acquisition cost is a strong function of the sustainment costs associated with fielding and maintaining an electronic system. Military equipment usually have operational lifespans of over 20 years. During this lifespan many systems of the electronic equipment structure wear out dictating a strategy for their replacement or refreshing during their life. In order to reduce the cost associated with fielding and maintaining of electronic system, program managers must have an understanding of the life expectancy of the electronic system and must be assured that the electronic system can meet the necessary life cycle requirements. Further, methods must be in place to allow engineers to make these risk assessments in a timely manner with minimal trial and error. The fundamental goal of an up-front product qualification using simulations is to provide an analysis in parallel, rather than in serial and to allow the designer to be able to deliver in-process design changes sooner.

Virtual life assessment is a failure prediction methodology based on the scientific determination of the dominant failure mechanisms and failure sites within the electronic component. The dominant failure mechanisms and failure sites are exposed by characterizing the stresses in the system using thermal or vibration analyses as inputs for analytical models derived from physical phenomena fundamental. Most of the time these physical processes from where the analytical models are developed are chemical, metallurgical, physical, or thermo-dynamical in nature.

The virtual life assessment differs from more traditional reliability prediction or estimating techniques because the prediction can be made at the design stage; rather than based on field and test data. The objective of accelerated product qualification is to assess whether a product will meet the application life requirements. Historically, this objective has been achieved by physical tests, sometimes referred to as accelerated stress tests (AST). Unfortunately, the application of AST does not necessarily guarantee field reliability (Caruso and Dasgupta 1998). Of particular concern is the possibility that failures precipitated during the physical test may not occur in the field (Chan and Englert 2001). More important, even if relevant failures can be precipitated, a quantitative technique is needed to extrapolate results from test conditions to life conditions. Thus, validity and usefulness of AST is brought under scrutiny. To address this problem, the virtual life assessment is used as an accelerated product qualification method. The fundamental barriers to effective integration of the virtual life assessment into a reliability prediction plan are: the cultural change that requires some

reliability analysis to be performed before/during the component placement phase, and the inability of current tools to provide all the needed data.

The input data required for the simulation method are environmental and operational profile conditions, which may include: power and voltage conditions, environmental exposures, duration and duty cycles at various temperatures, exposure to airborne contaminants, shock and vibration, humidity, radiation, maintenance, packaging, handling, storage, and transportation conditions. In addition to these inputs, material characteristics, damage properties, relevant geometries at failure sites, and manufacturing flaws and defects are necessary information. Variations in the input parameters account for the uncertainty of the model results. Other disadvantages of using simulation are the risk of non-valid results, which is uniquely dependent upon the validity of the underlying constitutive relations.

In general, analytical models are widely used to predict reliability, which have a power law structure (Englemaier 1993):

$$TCTF = Kp \cdot (\sigma)^{(\gamma)} \quad (1)$$

where TCTF is time- or cycles- to failure, Kp is a constant that depends on specific materials and product parameters, σ is a stress parameter, and γ a material parameter. This equation form provides an approach for prediction as well as for the interpretation of failure data. Most of the technical content for the analytical models are included in the technical references rather than in this paper (Dasgupta and Pecht 1991; Engel 1993; Frear et al. 1994; Liu and Qian 1998). However, these are not the only models; a significant number of theoretical models have been published in literature. These models are based on fracture mechanics approach, which define the number of fatigue cycles or time to propagate the dominant crack from an initial size to some critical dimension.

2 CASE STUDY

To demonstrate the virtual life assessment process, several electronic systems used in the United States Marine Corps (USMC)-Advanced Amphibious Assault Vehicle (AAAV) were reviewed and sufficient data to conduct virtual life assessment was collected for two circuit card assemblies (CCAs), the Input/Output and Analog Monitor CCAs. The exercise resulted in an assessment of the likely failure sites under the anticipated life cycle and test loads. The calcePWA™ software, developed at CALCE EPSC of the University of Maryland was used for this study. Osterman et al. previously used the software in the successful qualification of circuit cards in a military radio (Osterman and Stadterman 1999). The major drawback of their article was the low level of explanations used.

2.1 Assembly Information

The first step in conducting virtual life assessment was to develop a computer model of the hardware that is being analyzed. This model was developed from available design documents. The physical support structures for the CCAs were determined from a review of the CCA designs and discussions with USMC personnel. The two CCAs are housed in heavy metal enclosure, which provides physical support and protection. Within the enclosure, the CCAs are supported on two sides by wedge lock supports, a long bus connector to the backplane supports the bottom edge, and the top edge is simply supported by a top cover.

2.2 Load Characterization

After developing a model for the physical hardware, the expected life cycle load conditions to which the hardware will be subjected must be determined. For military applications, environment and operational conditions can be expected to be quite harsh (Steinberg 1988). In addition, mobile systems can be expected to experience random vibration, mechanical shock, and temperature cycling. Random vibration is caused by on-board engines as well as by the terrain over which the system is expected to traverse. Shock loads can occur due to explosive charges being detonated near the vehicle as well as from hard landings, other vehicle impacts, or gun firing. Temperature cycling can be expected to occur due to power cycling as well as thermal diurnal conditions. In addition, product quality assurance programs may also subject hardware to physical damage.

The life cycle and test stress profiles used in this analysis are presented in Table 1 based on information obtained from the USMC personnel. The life cycle stress profile was composed of individual stress segments. Each stress segment defined a specific loading condition with a specific application period and duration.

Table 1: Suggested Life Profile

Test Type	Stress Range	Duration
Temperature Cycle	125 – 0 °C 10 minute Tmax dwell 12.5 minute ramps 40 minute cycle	36 cycles/day
Random Vibration	0.04 G^2/Hz 100-900 Hz *	24 hrs/day
Shock	40g, half sine	11 msec

Simulations were conducted to determine the response of the CCAs to the anticipated temperature, random vibration and shock loading conditions. The temperature loads from the temperature cycle were assumed to be transmitted through the edges of the cards. Natural convection was assumed at the top and bottom surfaces of the circuit cards. As noted, the right and left edges of the cards were constrained by wedge lock supports that restrict translational motion and rotation. The top and bottom edges of the cir-

cuit cards were simply supported. The simple support assumption restricts translational motion at the support points but allowed rotational motion. The simple supports were selected to provide a conservative estimate. The selection of simple supports results in lower natural frequencies, hence bigger curvatures.

2.3 Failure Assessment

The failure mechanisms analyzed and the failure type identifiers are presented in Table 2.

Table 2: Failure Type Identifiers

Failure type	Failure site	Failure mechanism
Interconnect failure due to shock	J-lead and solder joint	Overstress
	Gullwing lead and solder joint	Overstress
	BGA ball	Overstress
	PGA pin and solder joint	Overstress
	DIP lead and solder joint	Overstress
Interconnect failure due to random vibration	Gullwing lead and solder joint	Mechanical fatigue
	J-lead and solder joint	Mechanical fatigue
	BGA ball	Mechanical fatigue
	DIP lead and solder joint	Mechanical fatigue
	PGA pin and solder joint	Mechanical fatigue
Interconnect failure due to temperature cycling	J-lead and solder joint	Thermal fatigue
	Gullwing lead and solder joint	Thermal fatigue
	Leadless solder joint	Thermal fatigue
	PTH barrel	Thermal fatigue
	BGA solder	Thermal fatigue
Conductive filament formation	Trace	Electrochemical migration

Damage induced by individual stress segments are quantified by the ratio of the number of cycles applied ($N^{applied}$) over the number of cycles that the structure can survive ($N^{available}$). Based on this assumption, the damage index for a single stress segment is defined as

$$D_i = \frac{N_i^{applied}}{N_i^{available}} \quad (2)$$

When considering multiple stress segments, the total damage index is defined as Miner's rule

$$D_{total} = \sum_i \frac{N_i^{applied}}{N_i^{available}} \quad (3)$$

Using cumulative damage (damage predictions of all the models are added and compare to the failure criteria (cumulative damage = 1)) as the failure criteria, failure is assumed to occur when D_{total} is greater than or equal to one. The life expectancy of the product is then determined by finding the time under the applied life cycle load conditions at which the worst-case damage ratio becomes one.

Table 3 presents life cycle failure assessment results for the defined life cycle profile for the two boards analyzed. Each potential failure site is listed by name and failure type that resulted in the highest probability of failure. The identified failure sites are listed and ranked in order of severity using the damage criteria of total damage obtained from Miner's rule. Using cumulative damage, when the total damage index reaches one (one was used as the failure criteria) for the stress profiles of the Analog Monitor and Input/Output CCAs the TCTF is obtained.

Table 3: Failure Assessment Results for Life Cycles

	Failure Site	Failure Type	Damage Criteria
Analog Monitor CCA at 6.5 years	U 112	Interconnect failure due to random vibration	0.98
	C 249		0.69
	C 243		0.65
	C 209		0.46
	C 180		0.46
I/O CCA at 7.5 years	C 100	Leadless interconnect failure due to temperature cycling	0.96
	C 101		0.96
	C 102		0.96
	C 41		0.96
	C 43		0.96

For the Analog Monitor board, random vibration was found to be the primary stress driver. Results for the first three natural frequencies and mode shapes indicated that the first modal frequency was above 400 Hz. In this case, component U112 was found to be a weak link, which is not entirely unexpected since U112 is a relatively large part (32 x 32 mm Plastic Quad Flat Package -PQFP) near the center of the board where there is a maximum out-of-plane curvature of 0.15 mil. The total application life time was found to be 6.5 years of continuous operation.

Using the above-mentioned approach on the Input/Output CCA, the analysis found an estimated life expectancy of 7.5 years of continuous operation. From this analysis, the primary failure driver was found to be temperature cycling. Component C100 and other large chip capacitors were identified as the weak links. It should also be noted that a suggested 40g, 11 milliseconds half sine shock load was found to be too severe for the Input/Output CCAs causing overstress failure of its components. Sensitivity assessment indicates that the shock load condition should be held below 36g's to avoid overstress failure.

An accelerated physical test was also simulated to precipitate the failures obtained from the virtual life assessment. The objective in the virtual test was to suggest a physical test that could be conducted in less than a month

that would produce relevant failures. Further, both random vibration and temperature cycling stress conditions were selected since life cycle loading conditions indicated significant contributions from both stress types.

When using the same boundary conditions of the CCAs used in the virtual life assessment to simulate the enclosure support structure, it was observed that failure sites shifted as the vibration load level was increased. This meant that only the temperature cycle could be modified to increase the test acceleration factor. Under these conditions, the maximum test acceleration factor was close to 100. This acceleration factor implies that a 10-year life cycle can be compressed to a test that can take over several weeks.

A review of the failure sites suggested that a change in test fixture design could be used to significantly increase the test acceleration factor. In this case, the support provided by the connectors was removed. This would require having free wiring connections, as opposed to rigid connections. Analysis of this situation indicates an approximate 50% reduction in the first fundamental frequency. With a PSD level of 0.04 G^2/Hz between 100 to 900 Hz, the maximum displacement of the CCA is expected to be approximately 5 mils. It should be noted that analysis results indicate a lower frequency and higher displacement response than would actually occur. This is due to the fact that the stiffness of the connectors would likely increase the actual natural frequency and reduce the actual displacement, but the desired effect would still be present under physical testing. A more accurate model of the connectors would be needed to support this claim.

The results of the virtual testing with this new configuration indicated a test acceleration factor of more than 300. This provides reasonable time compression while maintaining the same primary failure sites and mechanism. For this case, physical testing can be conducted in about a week. The failure analysis results are depicted in Table 4.

Table 4: Failure Assessment Results for the Test Cycles

	Failure Site	Failure Type	Damage Criteria
Analog Monitor CCA at 7 days	U 112	Interconnect failure due to random vibration	1.26
	C 249		0.62
	C 243		0.56
I/O CCA at 9 days	C 100	Leadless interconnect failure due to temperature cycling	0.99
	C 101		0.91
	C 102		0.85

3 SUMMARY

This study has revealed the potential of simulation tools in facilitating timely and cost-effective product qualification. Simulation identifies the critical design weakness, life-cycle design margins, optimal test setup, and acceleration factors for accelerated stress testing. In short, simulation guided qualification can reduce trial-and-error iterations and redesign efforts, product development time and cost, test time and cost. It can also improve confidence in product durability, facilitate supply chain management, and lower life-cycle supportability costs. The results can be used for logistics and maintenance planning.

In this paper, the physics of failure (PoF) virtual life assessment was presented and the feasibility of implementing the plan on electronic modules from the United States Marine Corp's (USMC's) Advanced Amphibious Assault Vehicle (AAAV) was examined. While the need to verify the PoF approach on an existing system for which USMC or their contractors have adequate field failure history and accelerated stress test data was discussed, no existing system was found to have adequate information. In view of the demonstrated effectiveness of the PoF method on other military hardware (GRCI 1998), it was decided to apply the method directly to next generation AAAV electronics.

Based on available data, the results from the virtual life assessment exercise indicated a potential for insufficient design margins in both circuit card assemblies under consideration. Specific concerns were raised over the ability of the Input/Output CCA to withstand shock load conditions. Further, failure due to wearout interconnect fatigue mechanisms based on anticipated temperature cycling and random vibration loading conditions suggests life expectancies of 7.5 years for the Input/Output CCA and 6.5 years for the Analog Monitor CCA. These values given for failure time are for $N_{50\%}$. There is the capability to calculate lifetime distributions if the Weibull parameters of the assembly process are known. As a general guideline, previous studies (Mawer 1996) on plastic ball grid arrays have shown that $N_{1\%}$ can be as much as 60% less then the number of cycles needed to reach $N_{50\%}$. It also should be pointed out that the life cycle loads considered nearly daily operation of the equipment. In addition, the virtual life assessment study did not include quality of workmanship, manufacturing process issues and stresses incurred due to handling and assembly of electronic systems during installation and maintenance.

Based on the virtual life assessment results, a test plan was developed for conducting accelerated product qualification through physical tests. The process of virtual testing facilitated the test plan. From the virtual testing study, test acceleration factors of above 300 can be expected for both CCAs with an anticipated test time of approximately one-week. Conducting the actual physical test would require several test articles, diagnostic equipment for functional monitoring the CCA during the testing, and software to accompany the diagnostic equipment for the individual CCAs. Participation from the product vendors and systems integrators would be a critical requirement. Conducting

the entire physical test would require test vehicle construction and characterization, step stress testing to determine physical operational and destruct limits, and accelerated stress testing. In addition, root cause analysis of failed test article would need to be conducted to identify failure sites. While the actual test may be conducted in about a week, the implementation of the entire physical test would take longer because of test setup and data reduction tasks.

From this exercise, the virtual testing effort using simulation techniques was demonstrated to be an effective method of developing physical tests. This process allowed the test developer to continuously monitor likely failure sites while varying stress levels and conditions. The obvious benefits are the speed with which the suggested test conditions can be simulated and iterated, and the ability to "observe" possible shifts in failure sites and mechanism. It also should be pointed out that the life cycle loads considered nearly daily operation of the equipment. Concerns not addressed directly by this virtual life assessment study include quality of workmanship, manufacturing process issues and stresses incurred due to handling and assembly of electronic systems during installation and maintenance.

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